RÉPUBLIQUE FRANÇAISE
Liberté Égalité Fraternité

FLEXGUARD: FAST MUTUAL EXCLUSION INDEPENDENT OF SUBSCRIPTION

→ → → TO APPEAR AT SOSP '25, SEOUL, SOUTH KOREA

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Background: blocking locks vs. spinlocks

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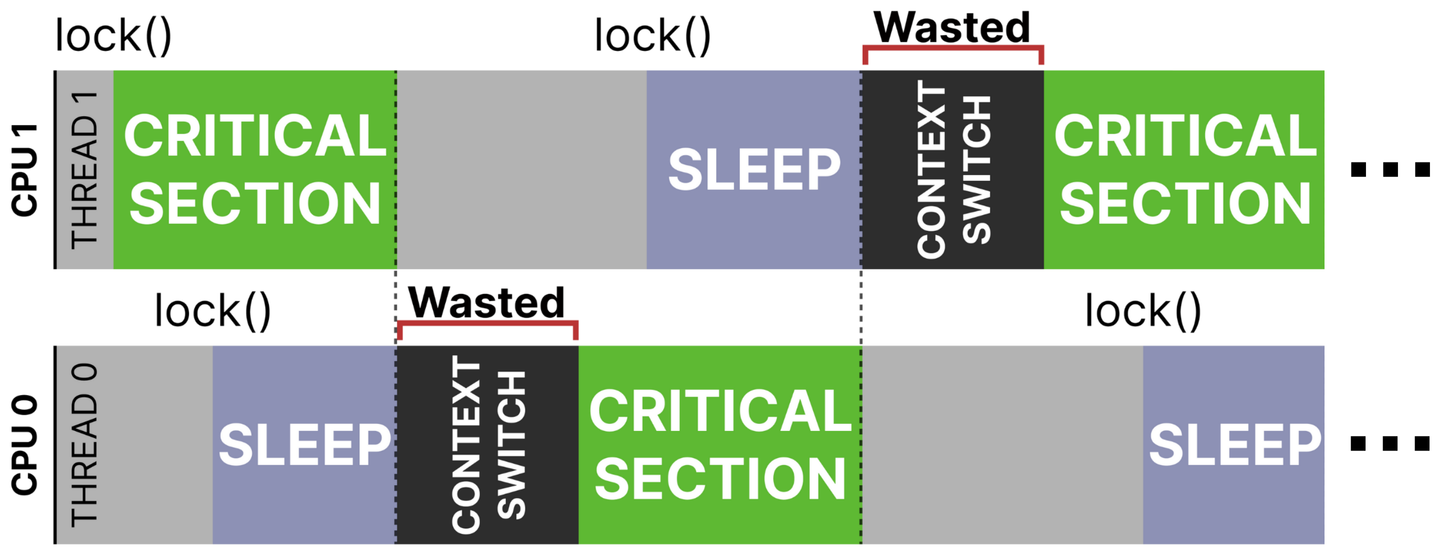

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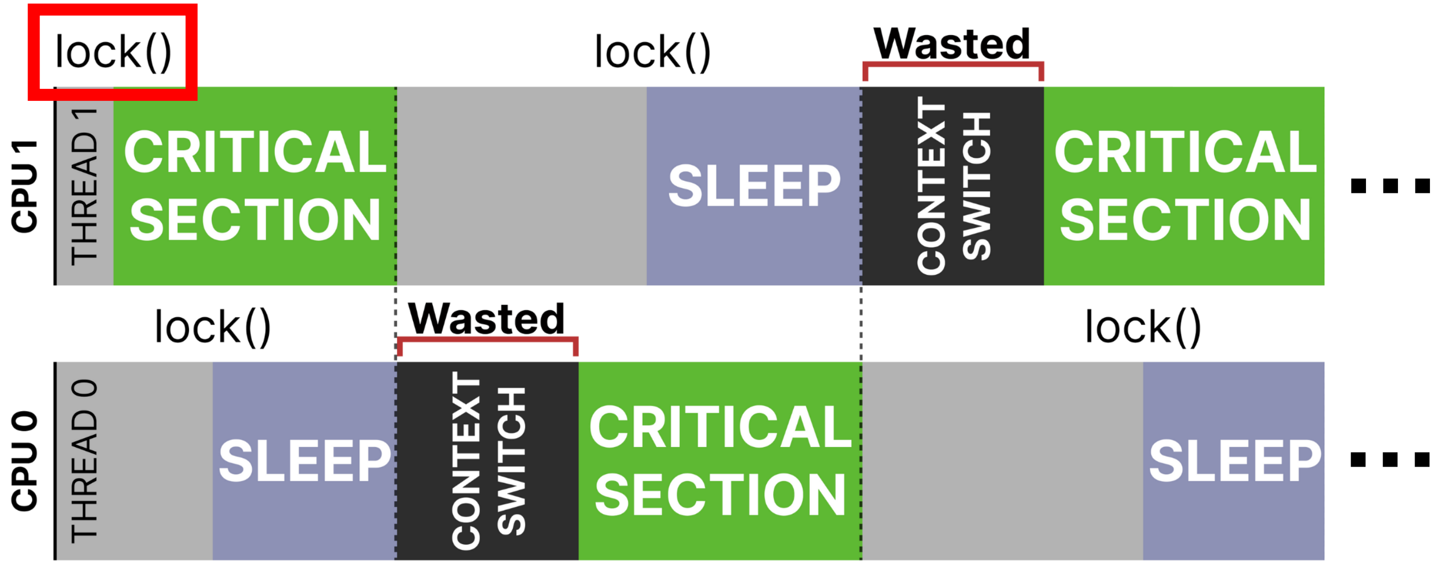

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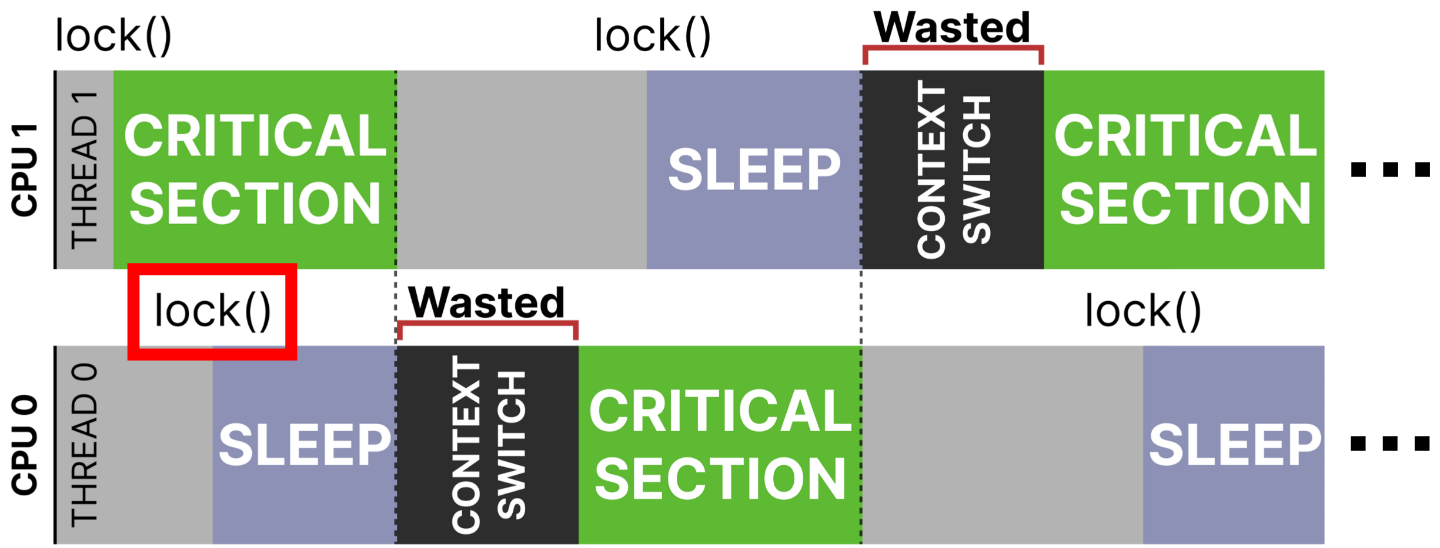

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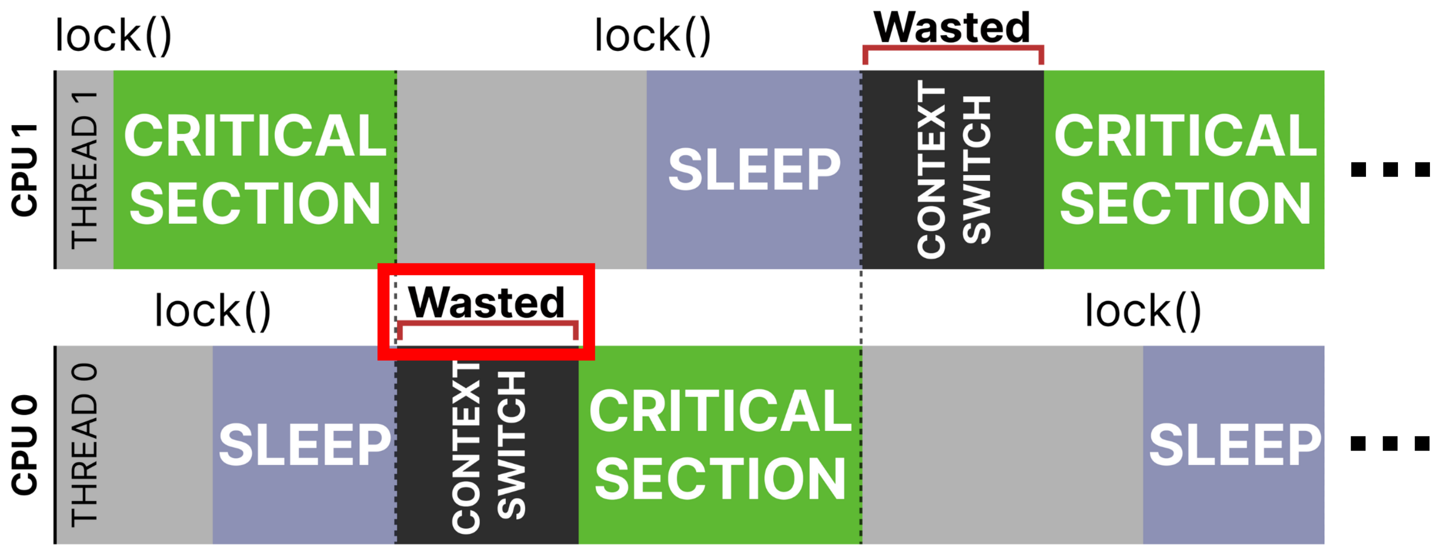

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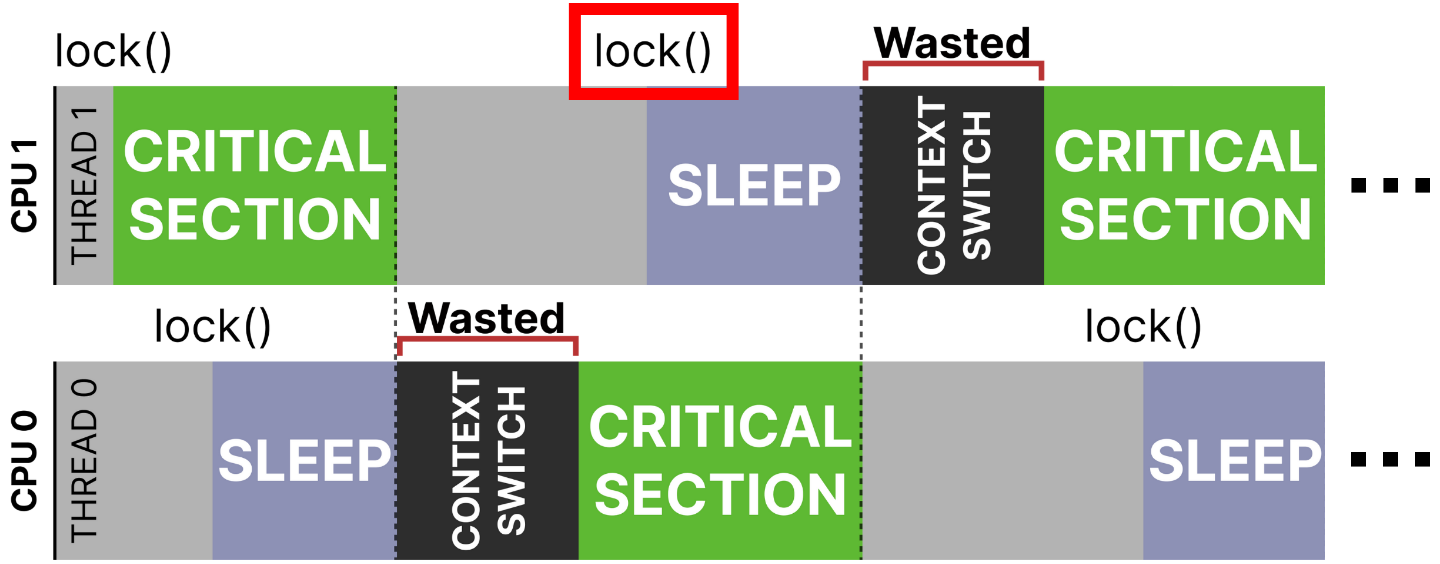

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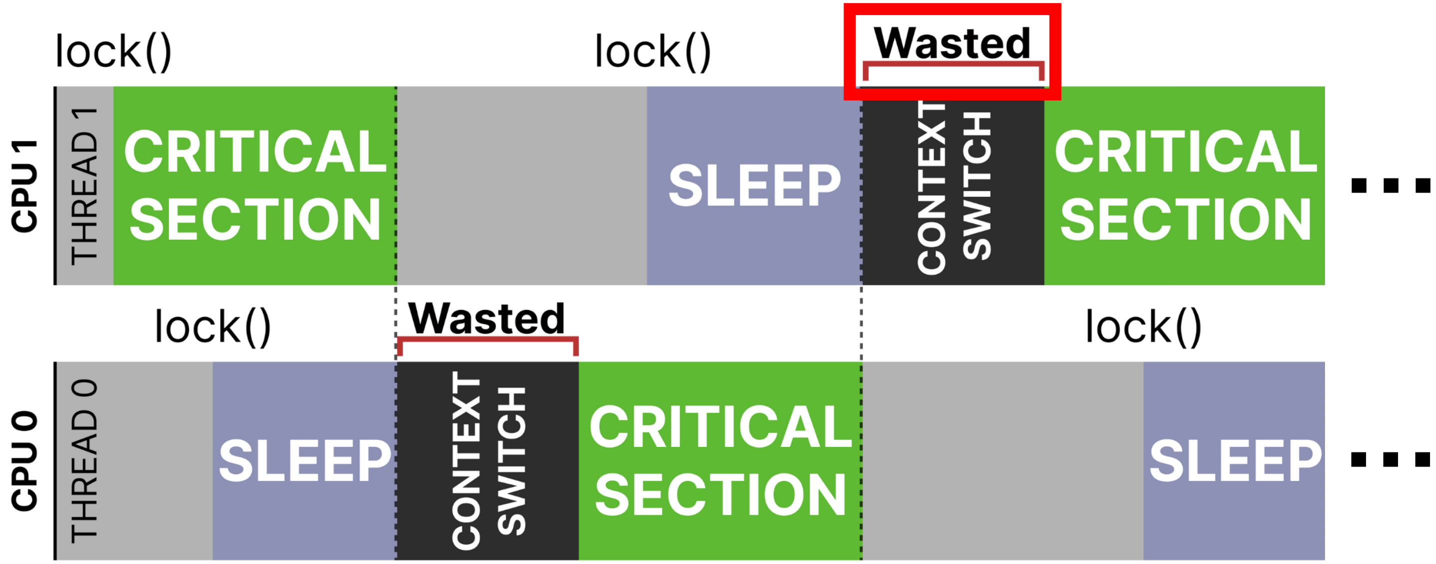

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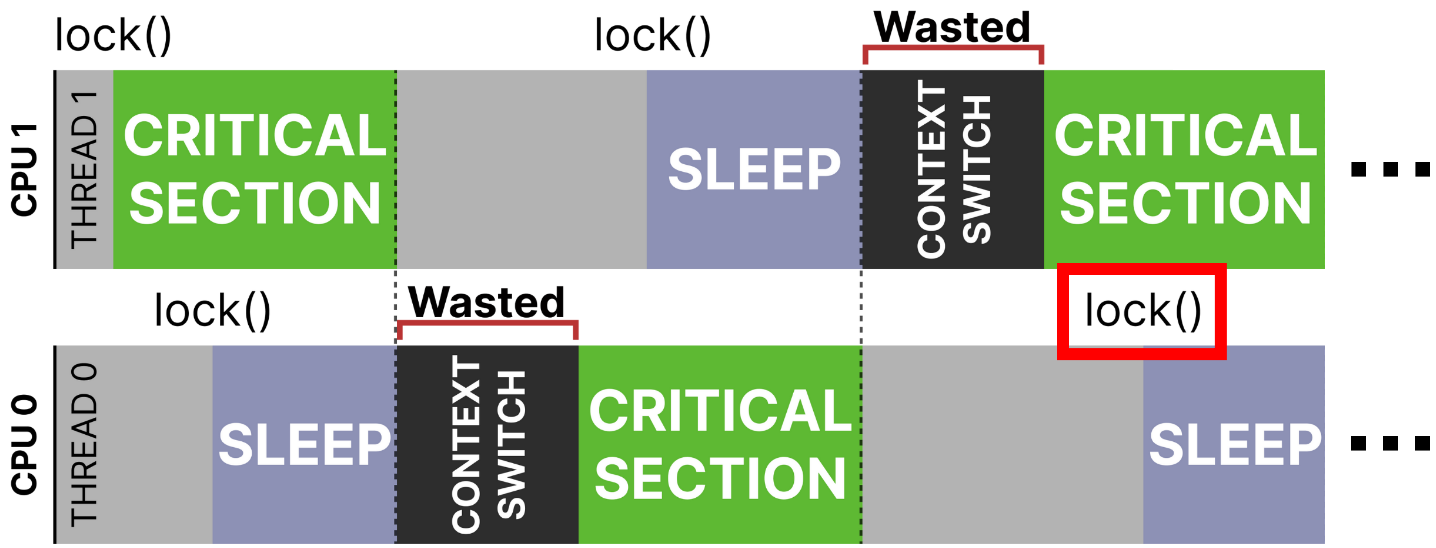

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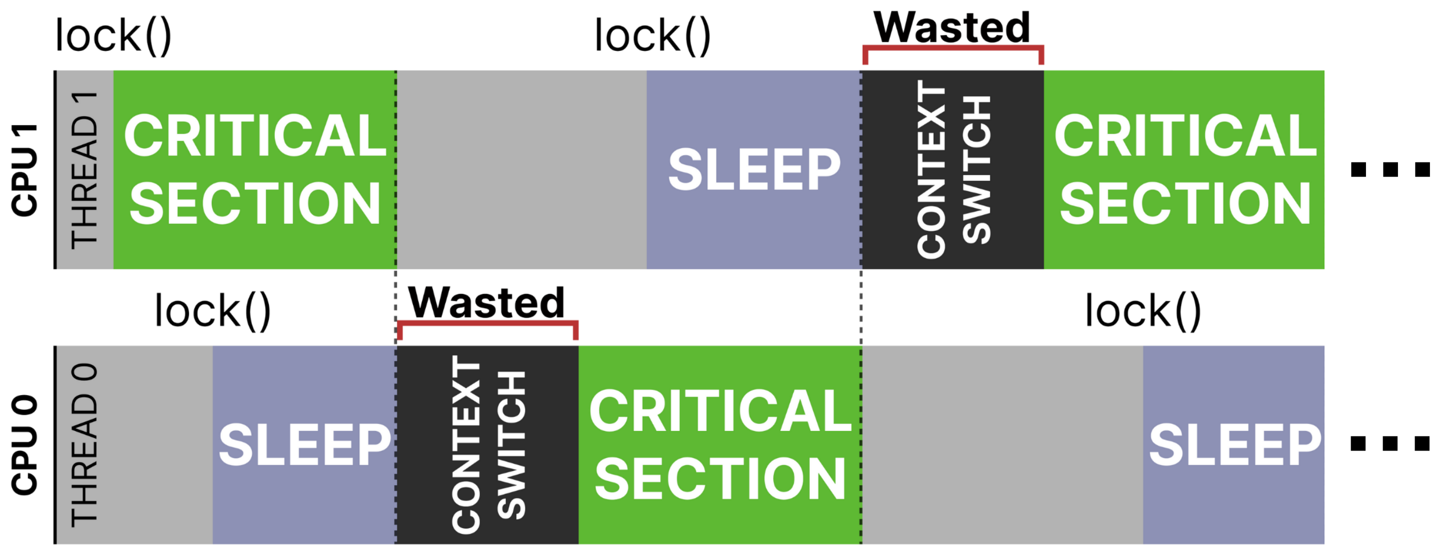

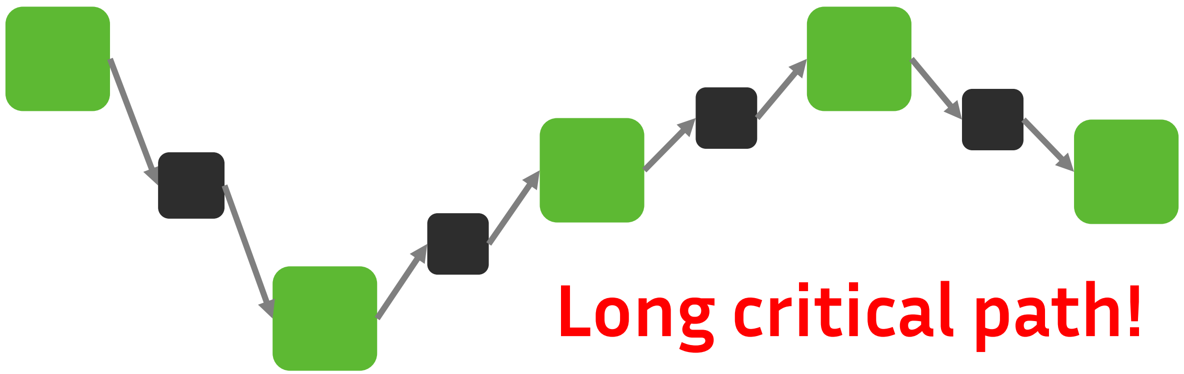

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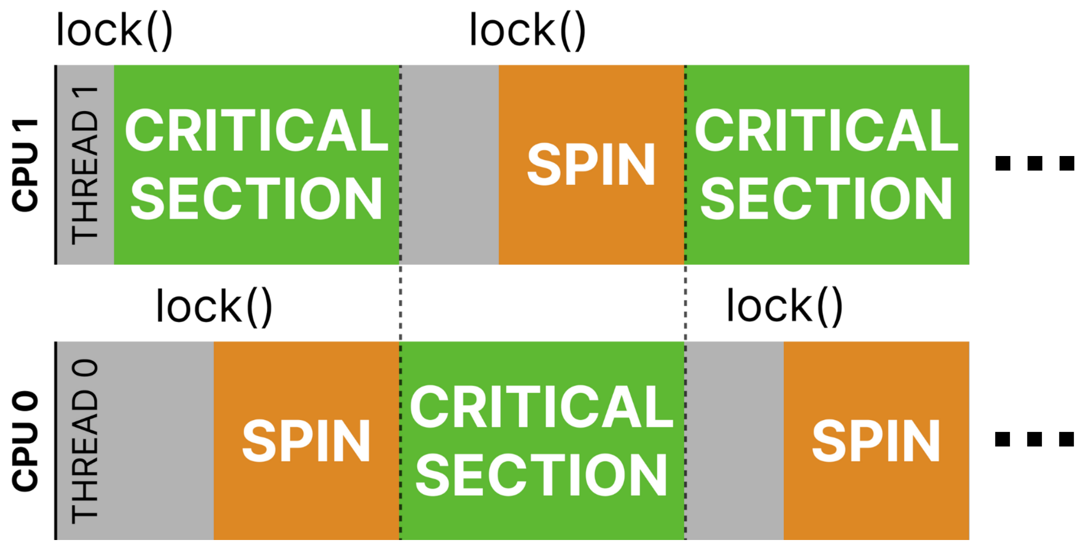

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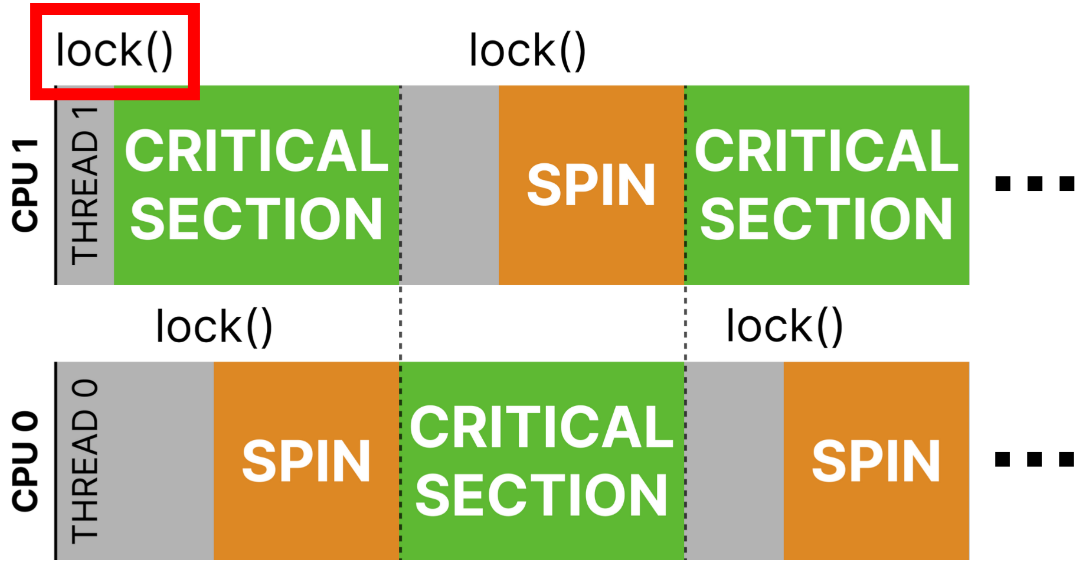

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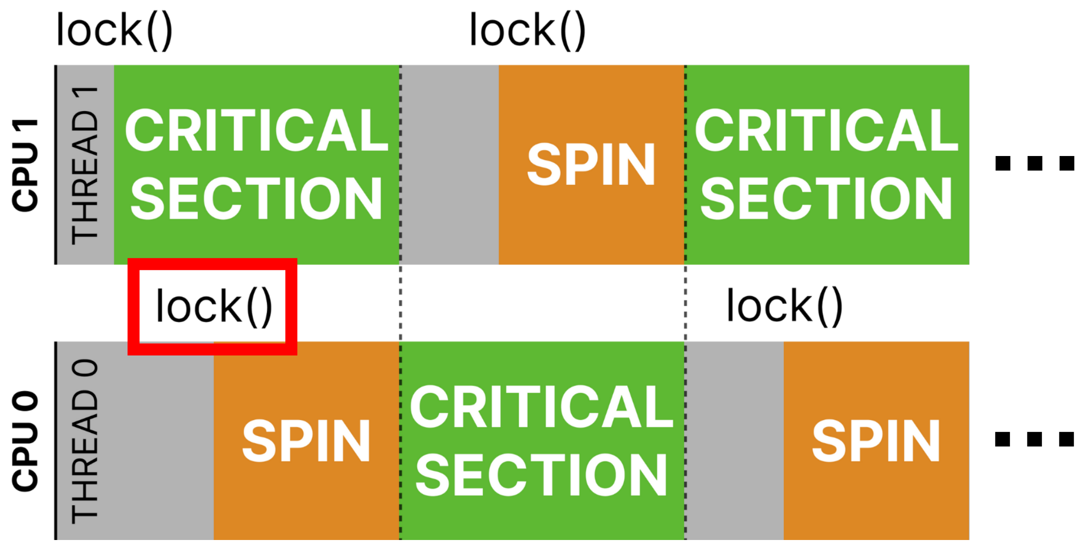

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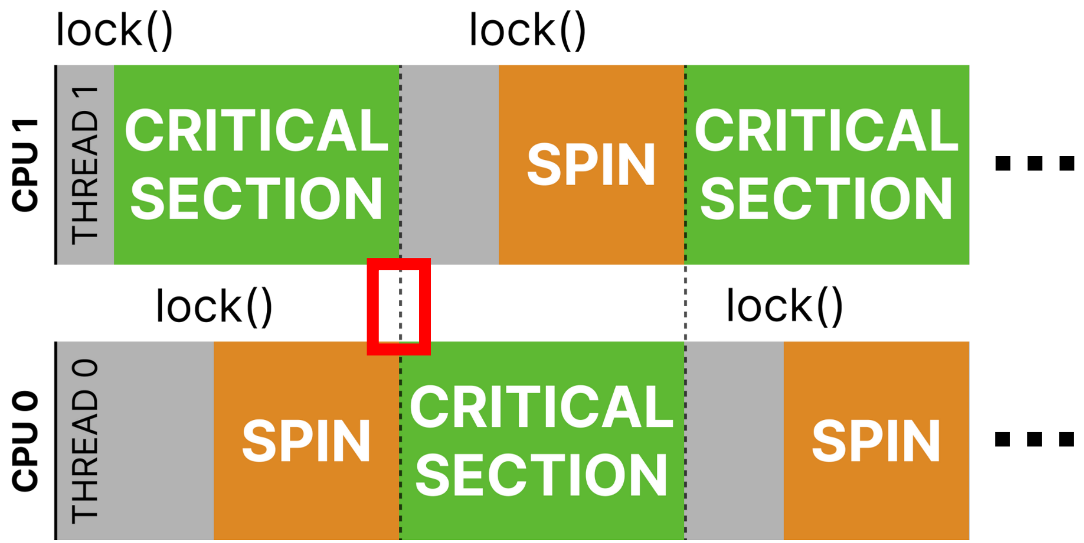

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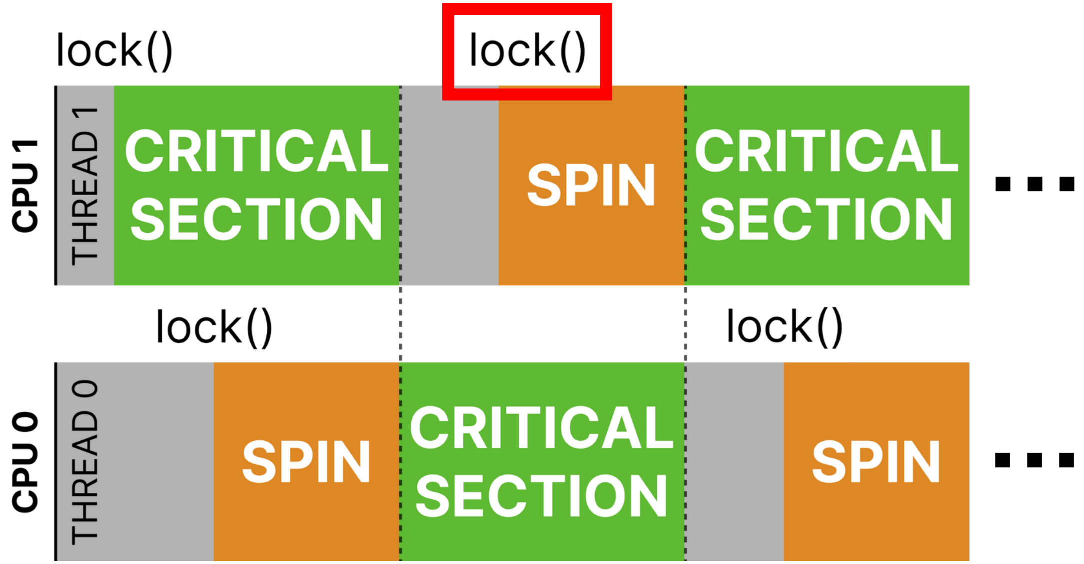

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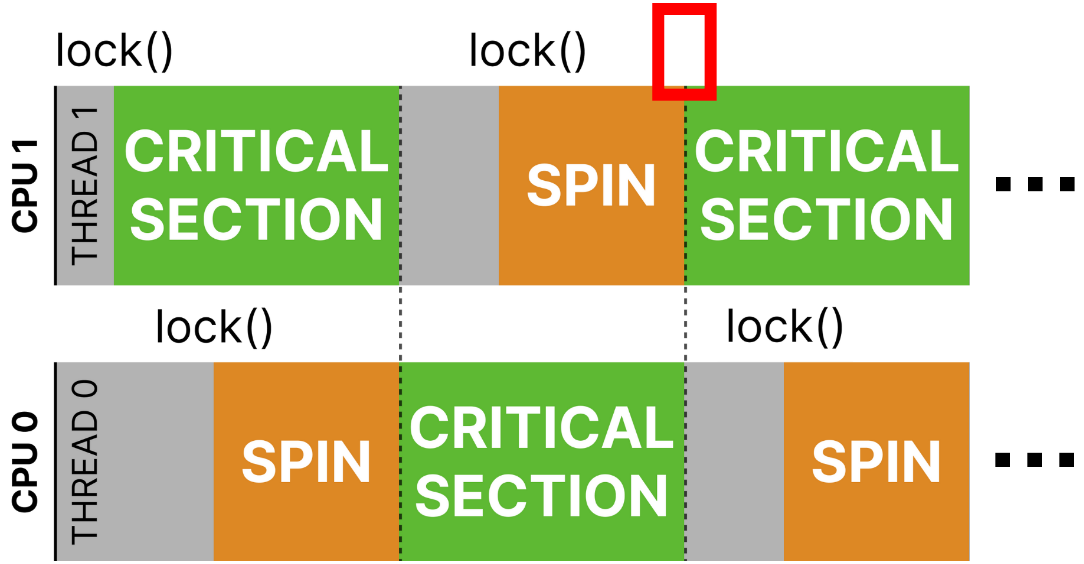

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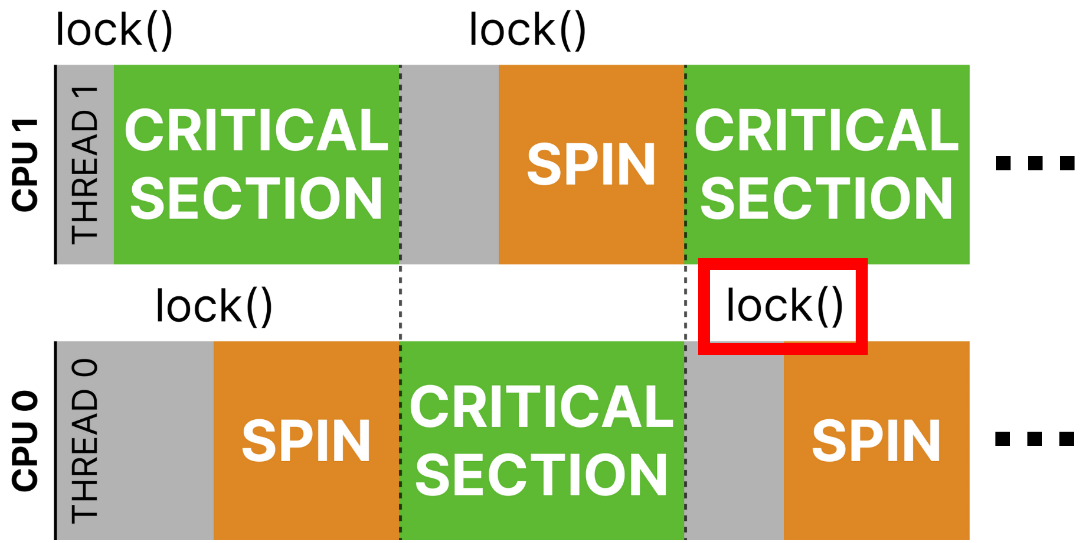

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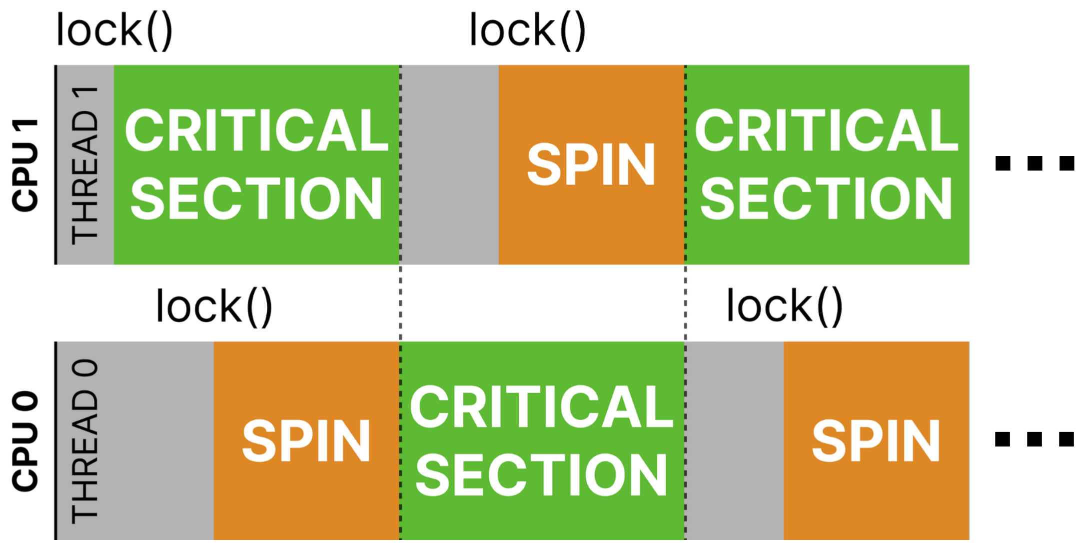

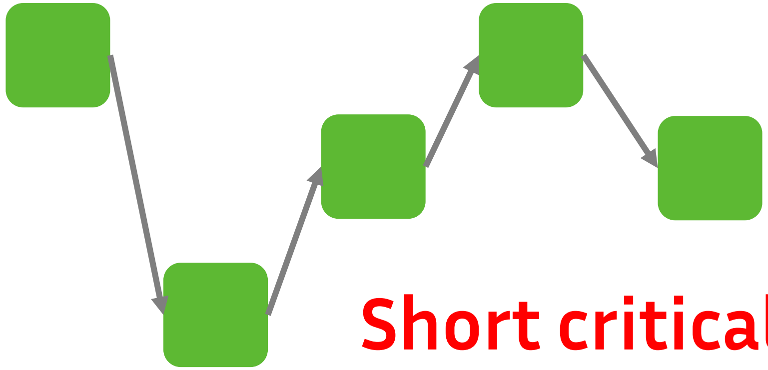

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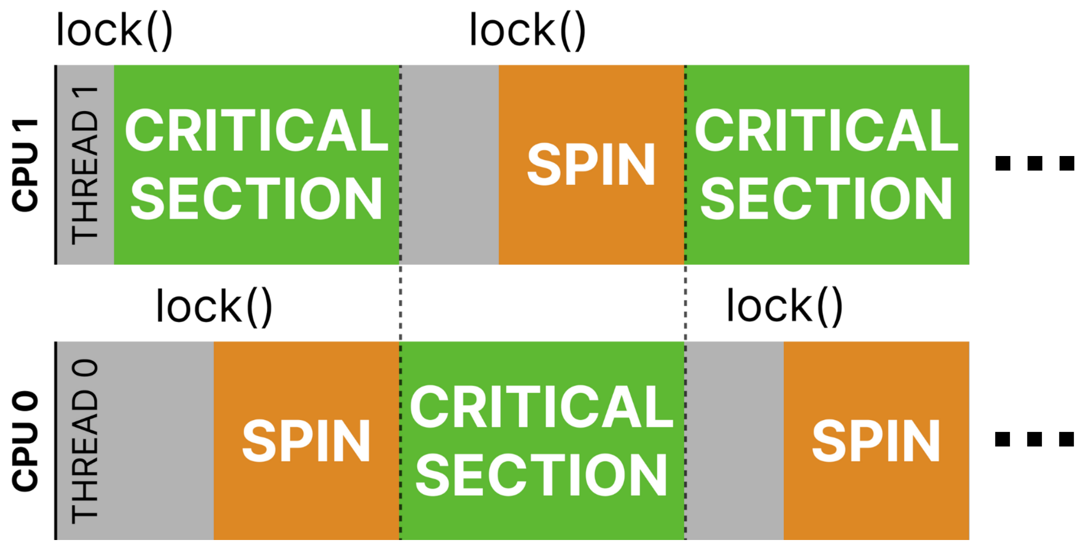

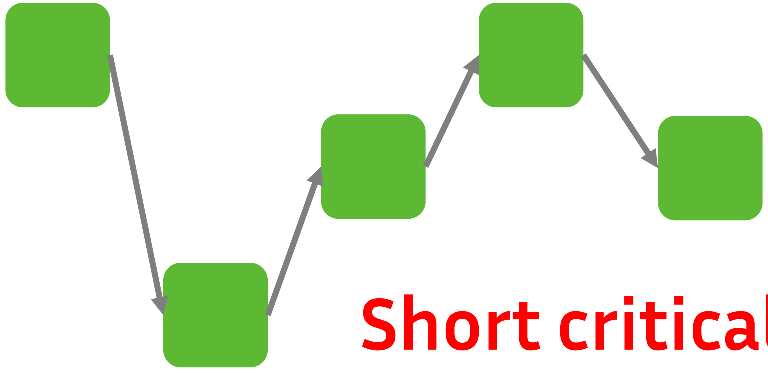

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- Spinning wastes energy? A few, but faster applications = lower energy consumption!

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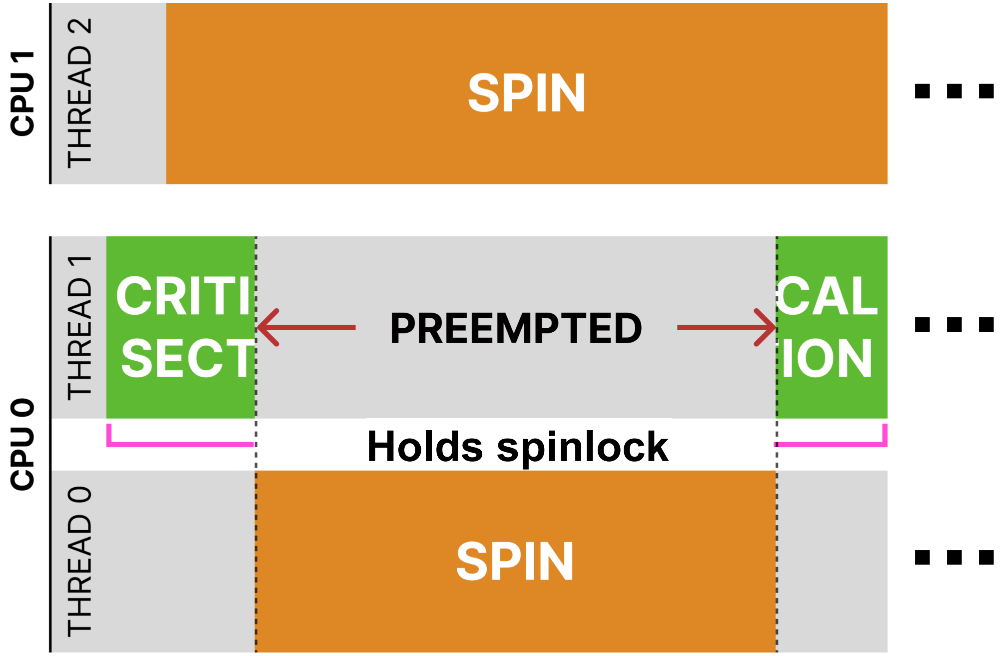

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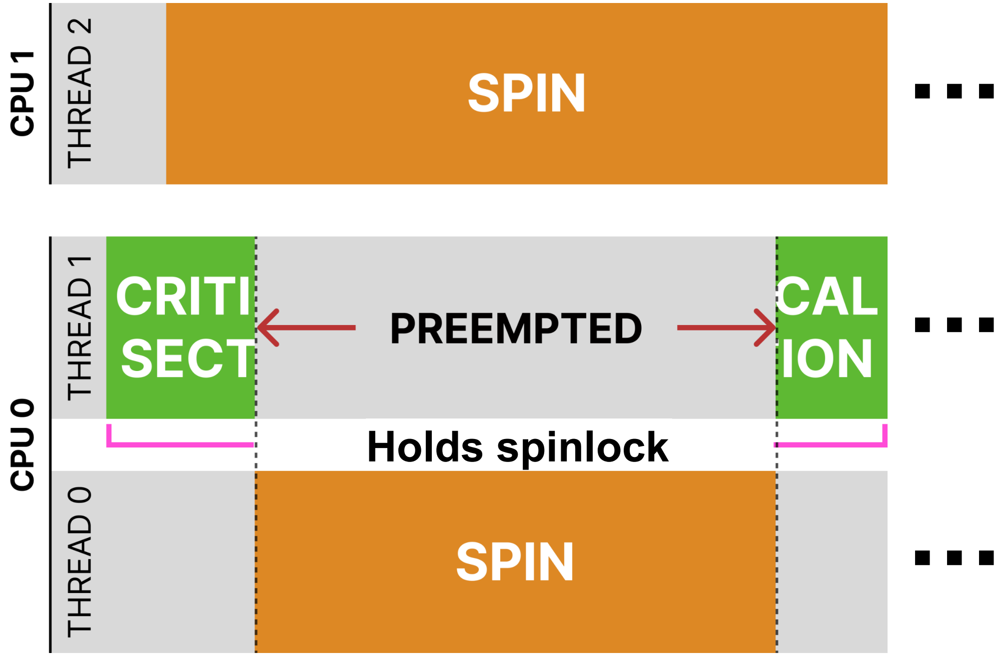

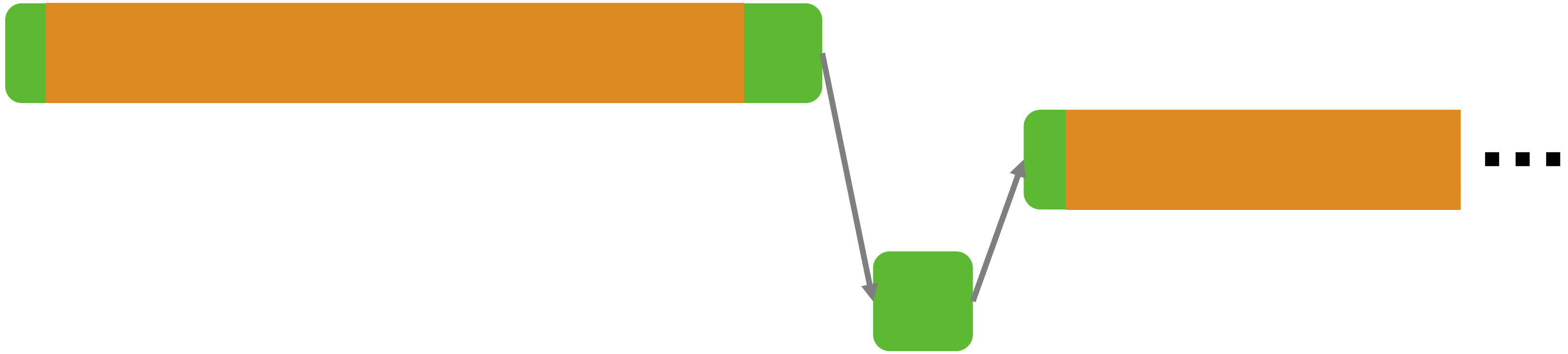

Extremely long critical path!

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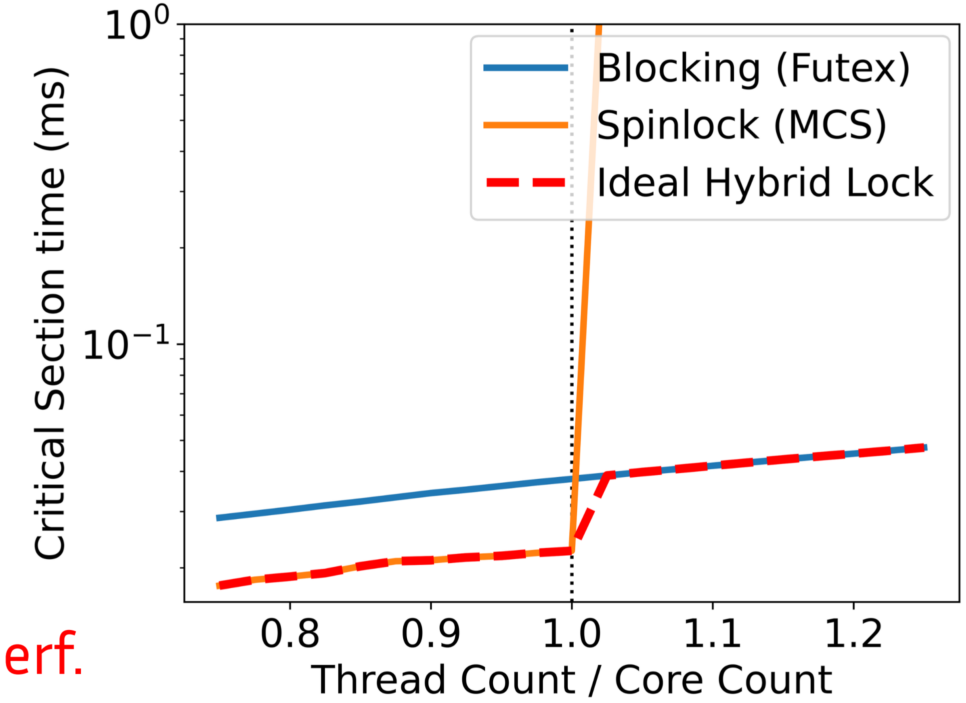

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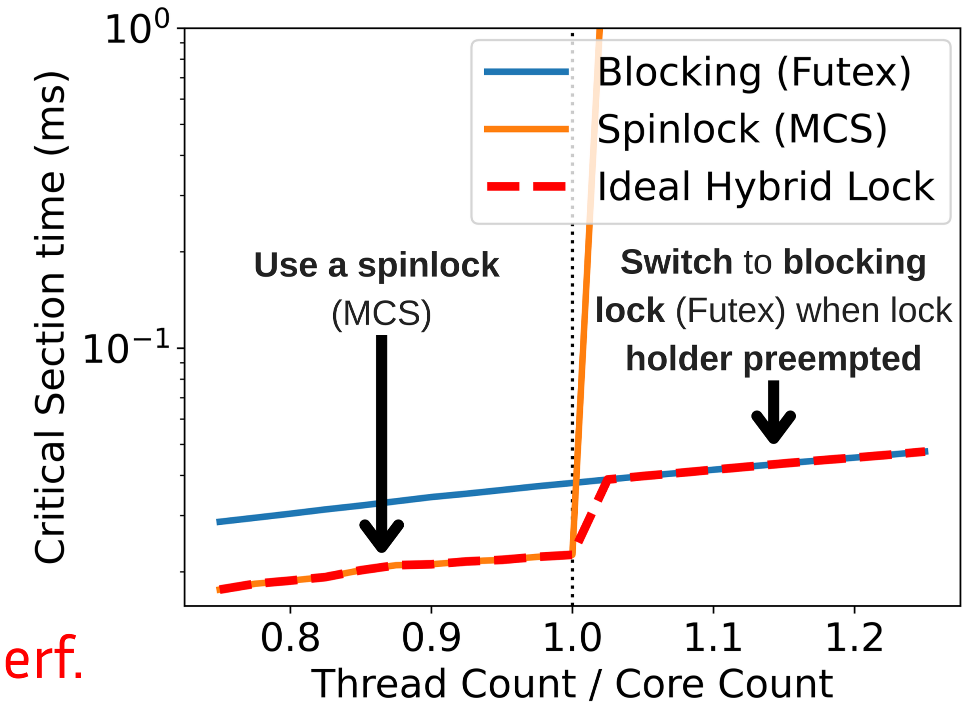

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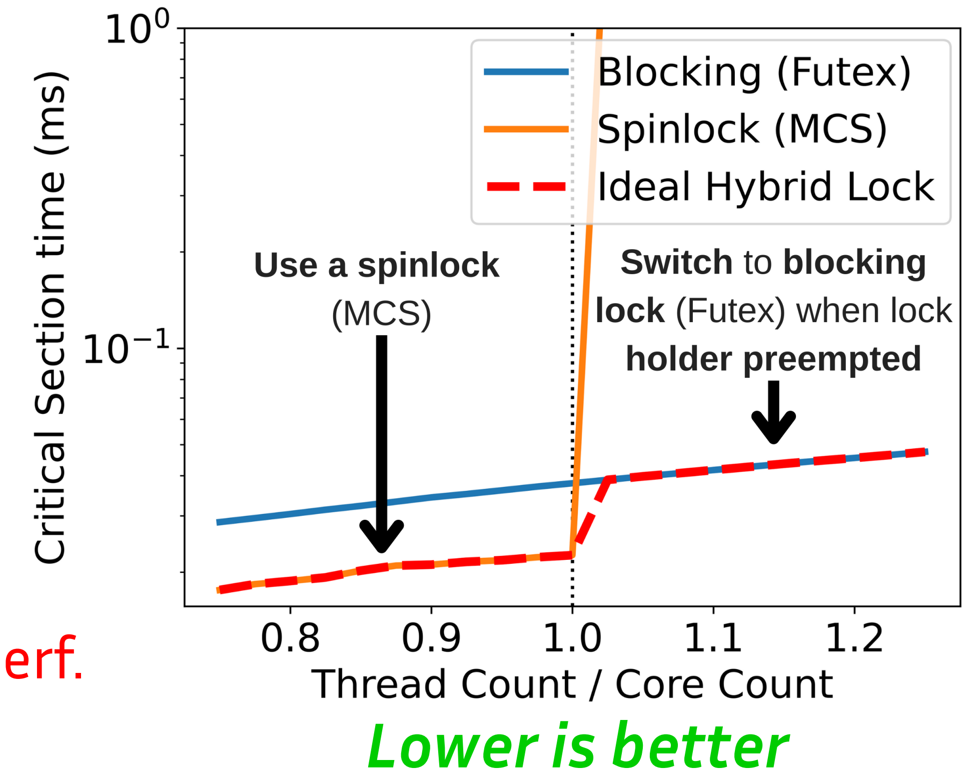

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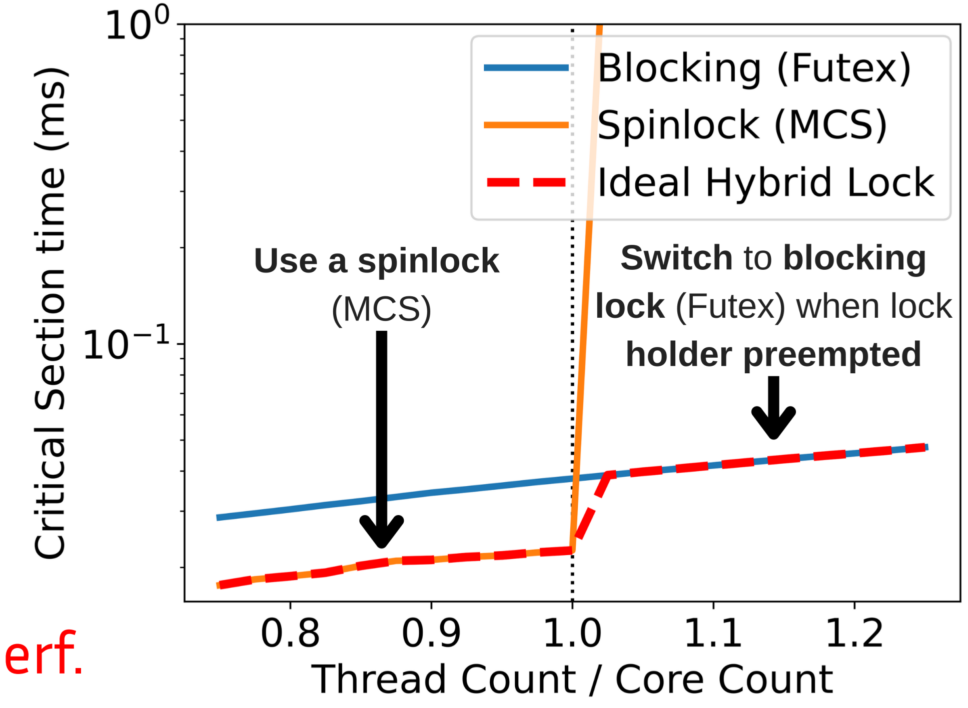

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  - Can we do this?
- **Insight:** nowadays, with eBPF we can!
  - We can instrument context switches to see all preemptions
  - We can view the full state of the thread: preemption address + register contents

⇒ We can 100% tell whether we are in a critical section!

eBPF

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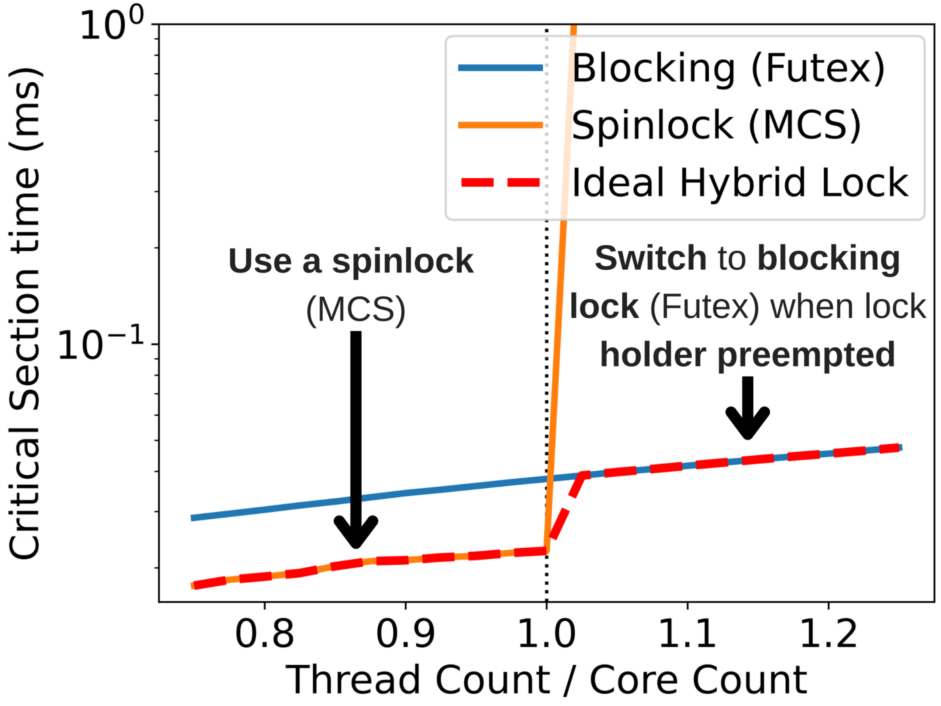

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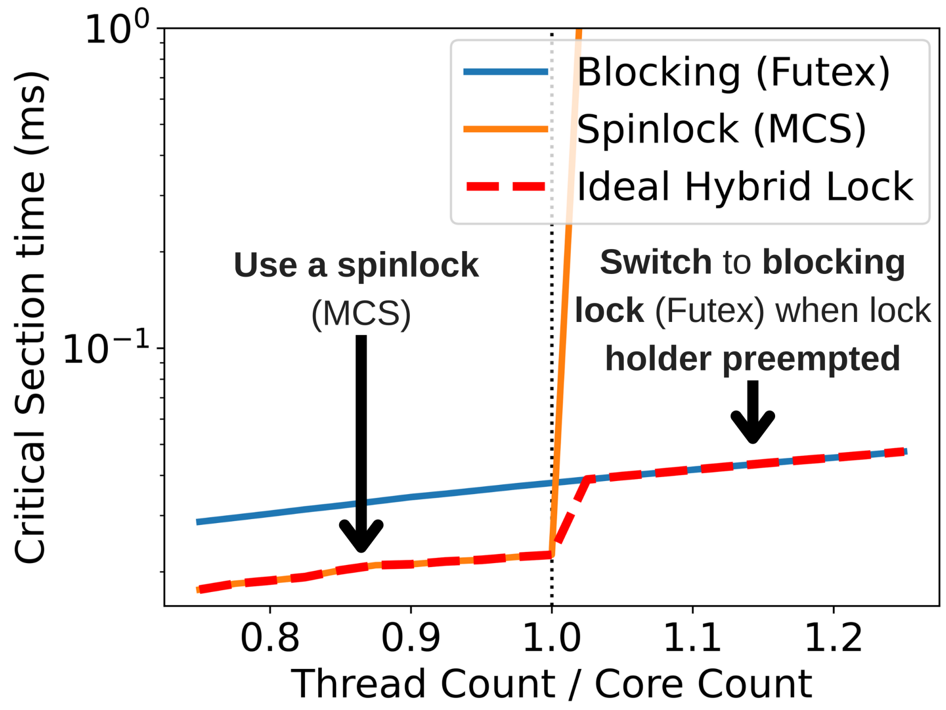

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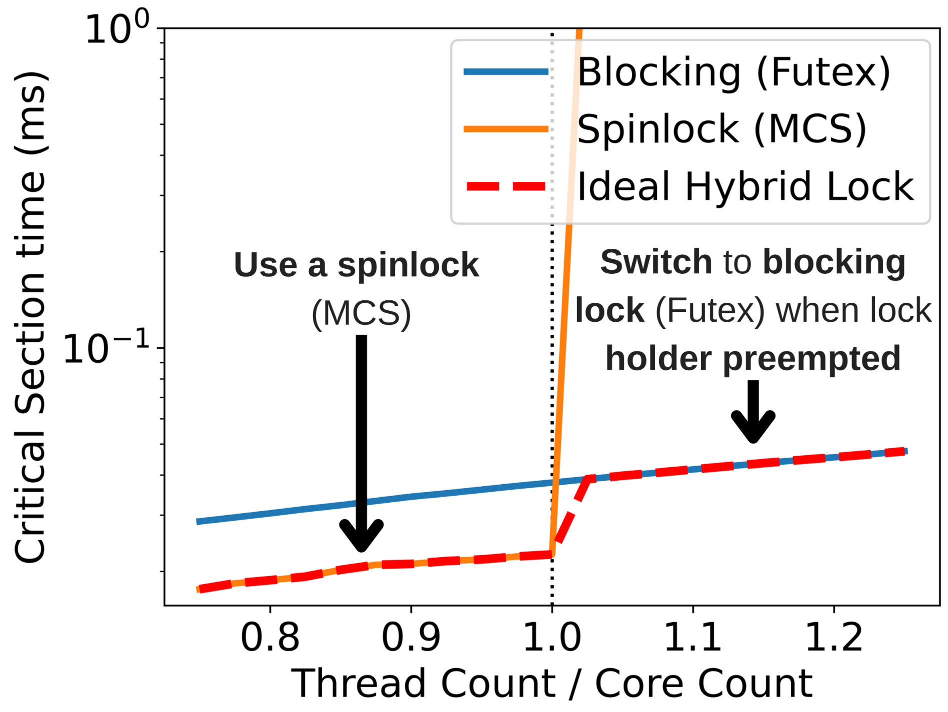

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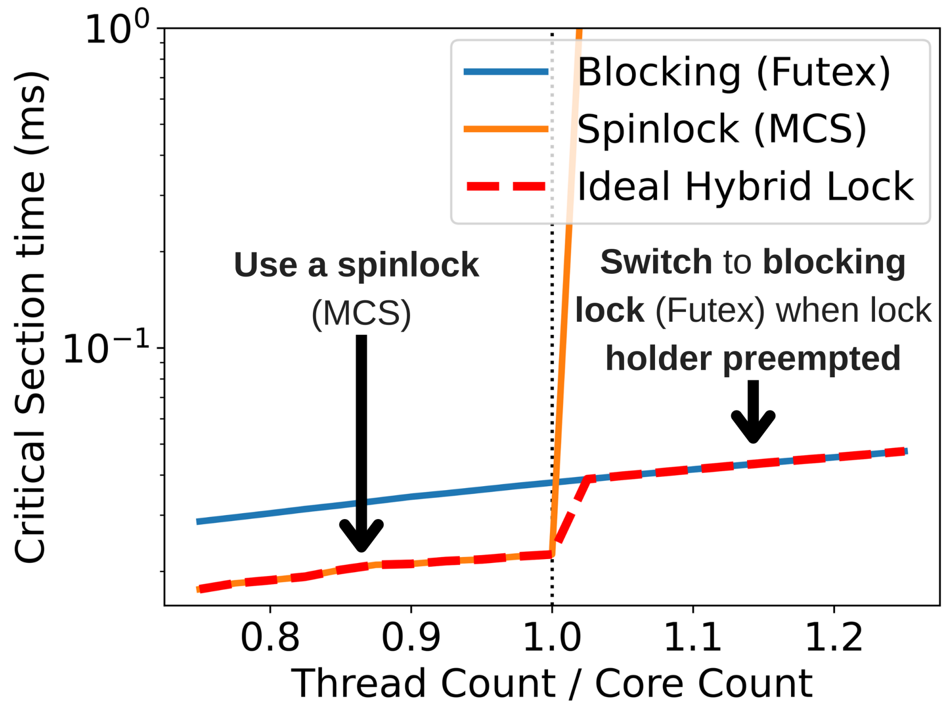

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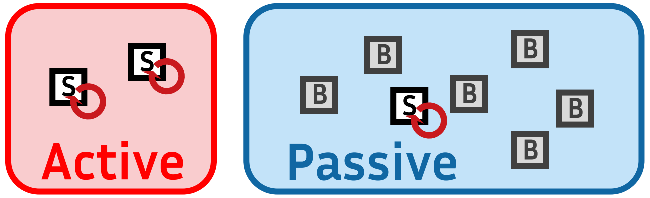

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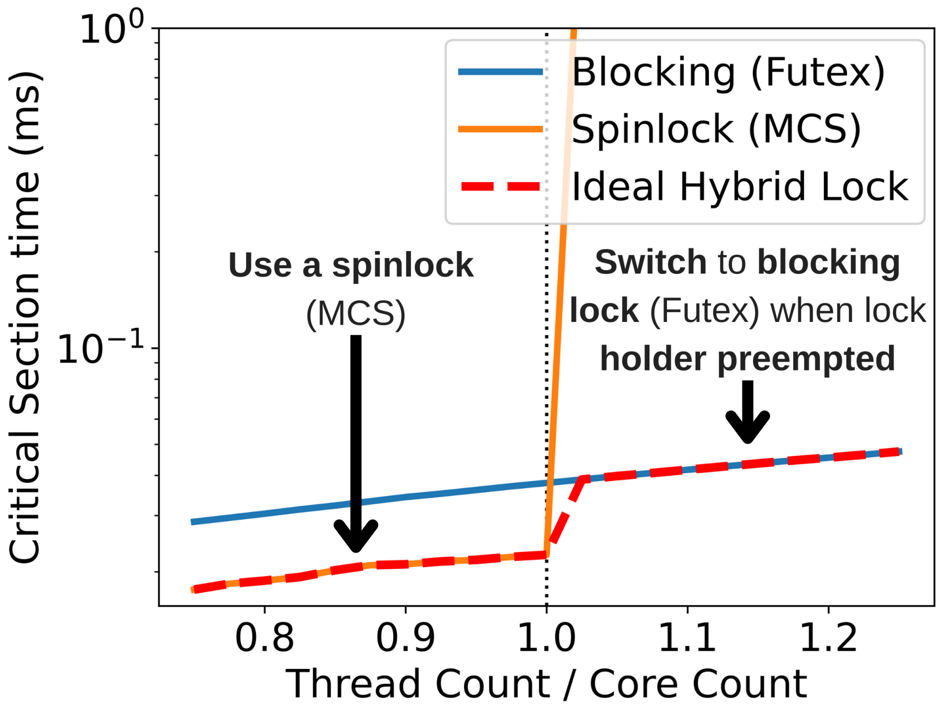

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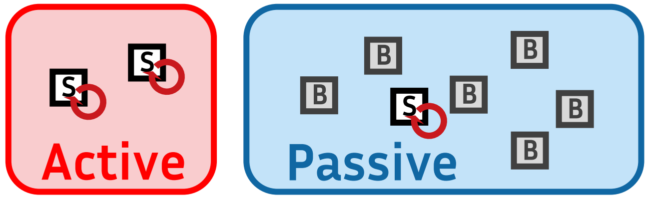
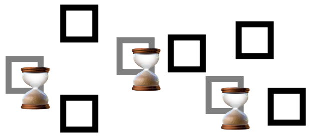
  - [He et al., 2005] **Time-published locks:** store timestamps, guess preemption if "stale" timestamp
    - **Heuristic:** what timeout do you pick?





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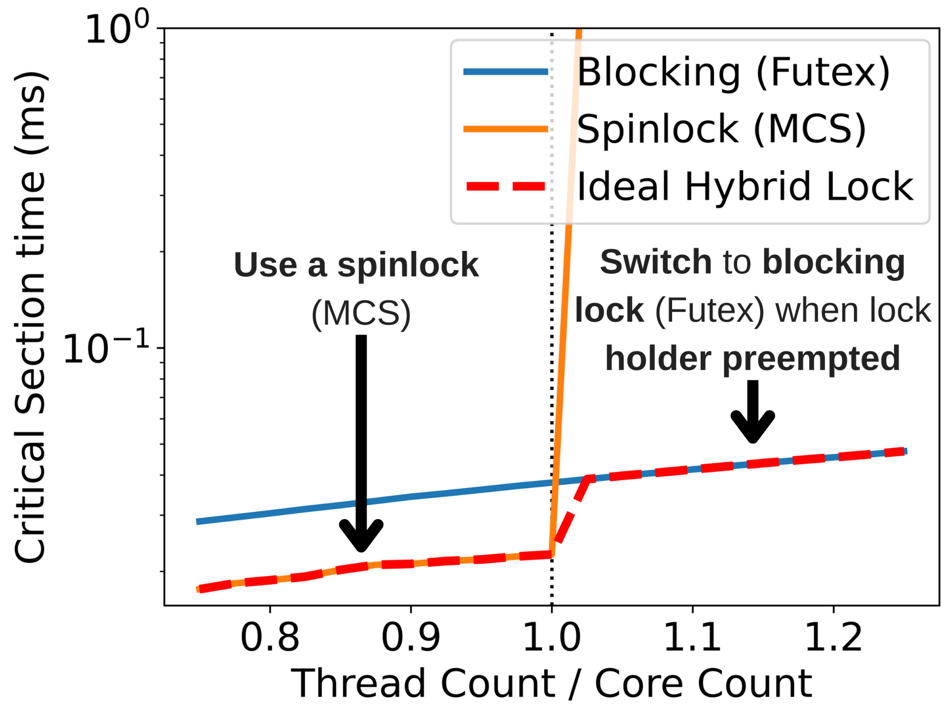
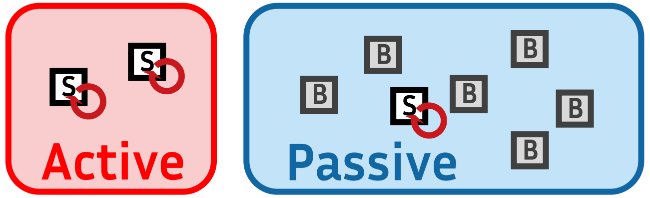


- Wait… Didn't others try to do this before?!
  - I.e., switch between spinning and blocking?
- **Answer:** yes, but they used unreliable heuristics!
  - **Spin-then-park:** spin a little before blocking
    - Actually POSIX uses this, sometimes worse than just blocking in our experiments
    - **Heuristic:** how long do you spin?
  - [Dice, 2017] **Malthusian locks:** spin-then-park + some threads in a "passive" list
    - Few active threads in the "spin" phase (fairness tradeoff)
    - **Heuristic:** how long do you spin?



  - [He et al., 2005] **Time-published locks:** store timestamps, guess preemption if "stale" timestamp
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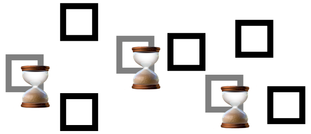
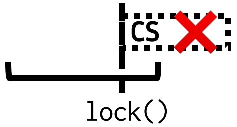


  - [Teabe et al., 2017] **I-Spinlocks:** only take the lock if enough time left in Xen timeslice (kernel locks in VMs)
    - **Heuristic:** how much is "enough time"?



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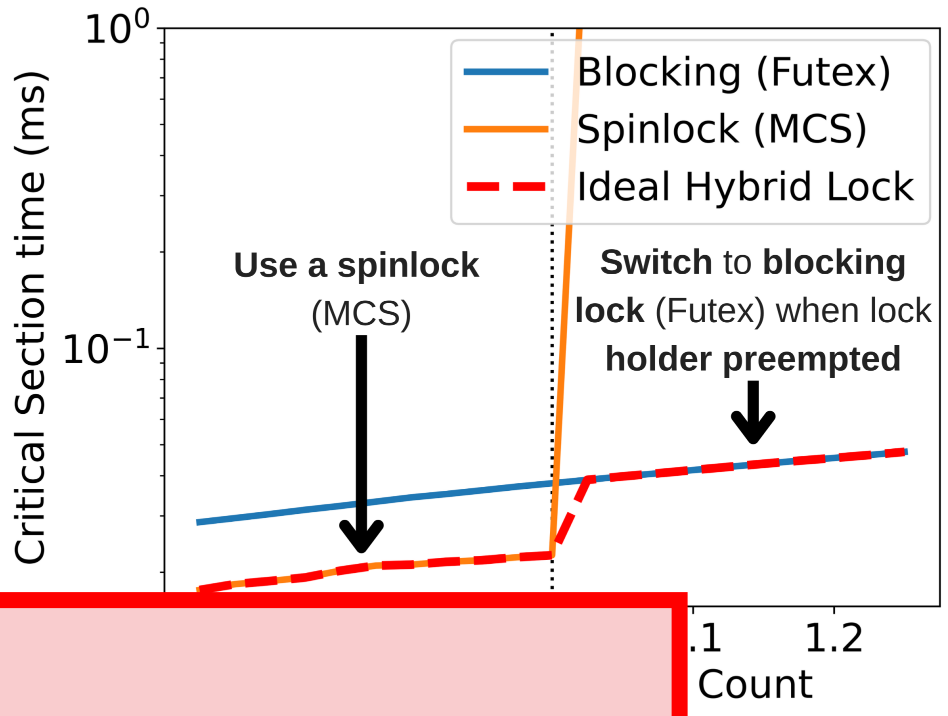

- Wait… Didn't others try to do this before?!
  - I.e., switch between spinning and blocking?

FlexGuard: first completely deterministic approach!
- Switches to blocking ***precisely*** when a critical section preemption happens
- Thanks to eBPF!

[Dice, 2017]
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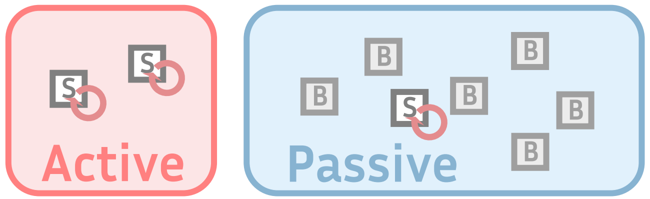

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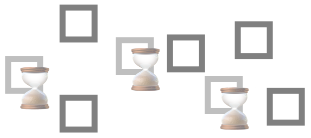

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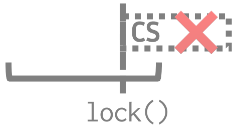

FlexGuard's Preemption Monitor

- FlexGuard's Preemption Monitor detects critical section (CS) preemptions
  - eBPF handler that hooks to the `sched_switch` event
  - **How to detect thread in a critical section?**

```
def lock(L):
  while (True):
    if L == UNLOCKED:
label at_xchg
      if XCHG(&L, LOCKED) == UNLOCKED:
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        break

def unlock(L):

label at_store
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  - **Idea:** use a flag!
    - Set it at the end of `lock()`
    - Unset it at the beginning of `unlock()`
    - If flag set, we're in a critical section!

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    - If `cs_counter > 0`, we're in a critical section

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eBPF

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    - If flag set, we're in a critical section!
  - **Actually, need to use a counter** for nested CSs
    - If `cs_counter > 0`, we're in a critical section
  - **Is that enough to be accurate?**

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CS

FlexGuard's Preemption Monitor

- **Answer:** no, the counter is not enough.

CS

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    - *There could be instructions until the actual* `cs_counter` *increment!*

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- **`unlock()` function:** when are we in the critical section?

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12   cs_counter += 1
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```

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- **`unlock()` function:** when are we in the critical section?
  - Until the store at line 16 actually completed, still in the CS!
    - *There could be instructions between the cs_counter decrement and that!*

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    - Assuming `at_store` is the final `MOV` that changes the lock variable's value

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    - Assuming `at_store` is the final `MOV` that changes the lock variable's value
- Can we take care of these cases?
  - **Yes, since the eBPF handler has access to the preemption address!**

FlexGuard's Preemption Monitor

- Is it finally accurate?

```
def lock(L):
  while (True):
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CS

CS

CS

FlexGuard's Preemption Monitor

- Is it finally accurate?
- **No, still one problematic case:**
  - What if preeemption right after the XCHG?
  - Then we are in a critical section iff the return value is UNLOCKED!

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CS?
CS
CS
CS

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```

CS? → if XCHG(&L, LOCKED) == UNLOCKED:

CS (label at_break … cs_counter += 1)

CS (cs_counter += 1 … cs_counter -= 1)

CS (def unlock(L) … label at_store)

- Is it finally accurate?
- No, still one problematic case:
  - What if preeemption right after the XCHG?
  - Then we are in a critical section iff the return value is UNLOCKED!
- Can we take care of this case?
  - Yes, we can force the return value of XCHG to be in a specific register (w/ `asm volatile`)
  - In the eBPF handler, we can access dumped register value (through the `task_struct`)!

  ⇒ Preemptions detected with 100% accuracy!

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- **Is it important to be fully accurate?**
  - Yes application critical sections only a few lines long, preemptions likely in `lock()`/`unlock()`
  - Sufficient to cause performance collapse!

FlexGuard's Preemption Monitor

```
__thread cs_counter = 0 # Per-thread critical section (CS)
                        # counter (# of CSs a thread is in)
__thread bool is_cs_preempted = False # Thread in CS?
num_preempted_cs = 0 # System-wide preemption counter
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```

CS

CS

CS

```
def sched_switch_btf(prev, next):
  # If next was previously preempted
  if next.is_cs_preempted:
    next.is_cs_preempted = False
    atomic_dec(num_preempted_cs)

  prev_in_cs = False # Will be set to true if prev in CS code
  if prev.cs_counter > 0: # values > 1 indicate nesting
    prev_in_cs = True # prev holding at least one lock; in CS
  else # prev.cs_counter == 0
    # Addr. of next instruction to execute after preemption
    preemption_addr = bpf_get_task_stack(prev)[0]
    if at_xchg < preemption_addr <= at_break:
      registers = bpf_get_task_registers(prev)
      if registers.rcx == UNLOCKED:
        prev_in_cs = True # lock acquired; already in CS code
    elif at_break < preemption_addr <= lock$end or
           unlock <= preemption_addr <= at_store:
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  if prev_in_cs:
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For communication w/ the lock

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next rescheduled in CS

Inria

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CS CS CS

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    atomic_dec(num_preempted_cs)

  prev_in_cs = False # Will be set to true if prev in CS code
  if prev.cs_counter > 0: # values > 1 indicate nesting
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      if registers.rcx == UNLOCKED:
        prev_in_cs = True # lock acquired; already in CS code
    elif at_break < preemption_addr <= lock$end or
         unlock <= preemption_addr <= at_store:
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  if prev_in_cs:
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FlexGuard's Preemption Monitor

```
__thread cs_counter = 0 # Per-thread critical section (CS)
                        # counter (# of CSs a thread is in)
__thread bool is_cs_preempted = False # Thread in CS?
num_preempted_cs = 0 # System-wide preemption counter
```

```
def lock(L):
  while (True):
    if L == UNLOCKED:
label at_xchg
CS?→ if XCHG(&L, LOCKED) == UNLOCKED:
label at_break
         break
  cs_counter += 1

def unlock(L):
  cs_counter -= 1
label at_store
  L = UNLOCKED
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CS (brackets: from at_break to cs_counter += 1; from cs_counter += 1 to cs_counter -= 1; from cs_counter -= 1 to L = UNLOCKED)

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prev preempted in CS

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- **For this, we need a bit of background on efficient lock algorithms**
- **Focus:** efficient spinlock algorithms
  - Blocking locks simply call the FUTEX syscall, can't be improved
  - *Unless you spin…*

Previous work on spinlocks

- **Basic spinlock**:

```
lock() {
    while (compare_and_swap(&lock, UNLOCKED, LOCKED) != UNLOCKED)
        PAUSE; // Spinloop hint
}

unlock() { lock = UNLOCKED; }
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  - `lock = UNLOCKED` invalidates `lock`'s cache line
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    - *Much faster than waking up a thread*
- In practice, spinlocks can be very fast, but you need smarter algorithms than that…
  - Lots of write contention on the `lock` variable!

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- **Optimisation 1: spin in read mode on the lock variable**
  - **Test-and-Test-and-Set (TATAS) lock**: test the lock value without an atomic instruction first

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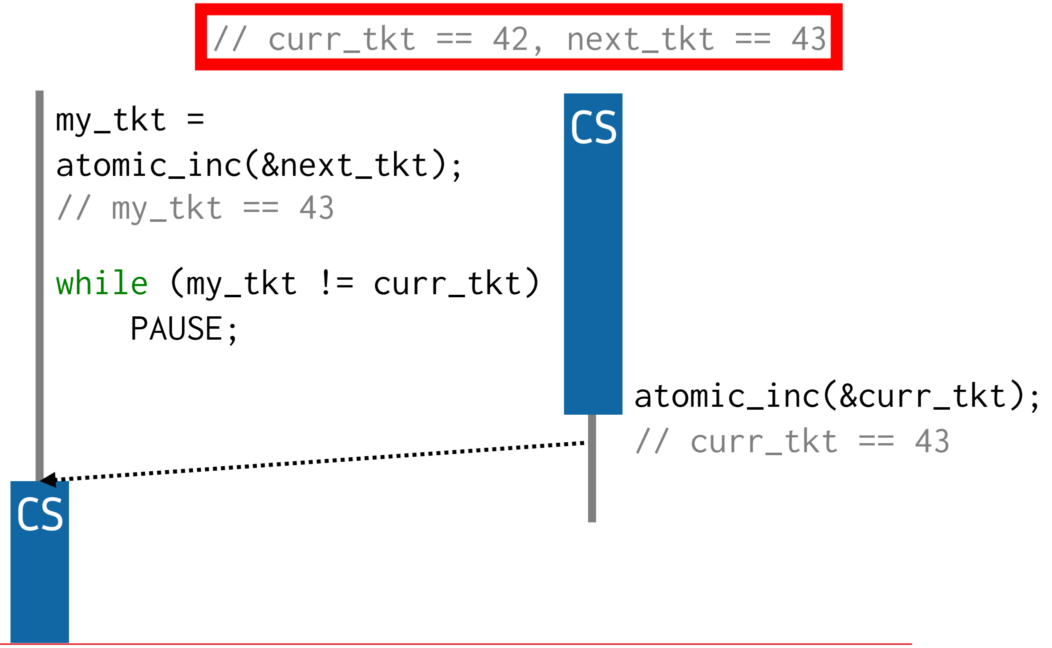

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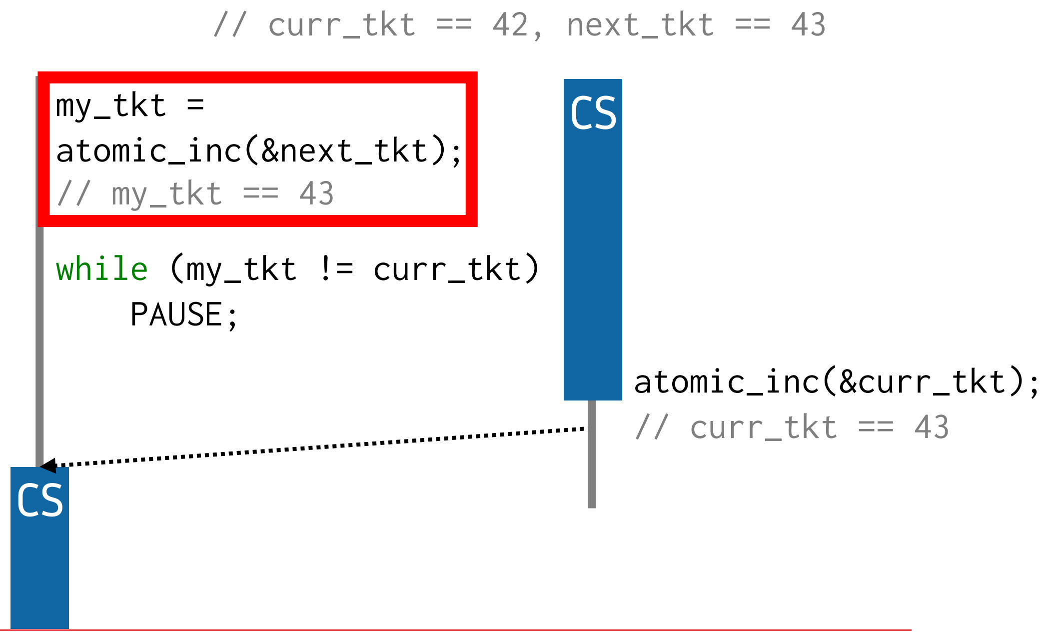

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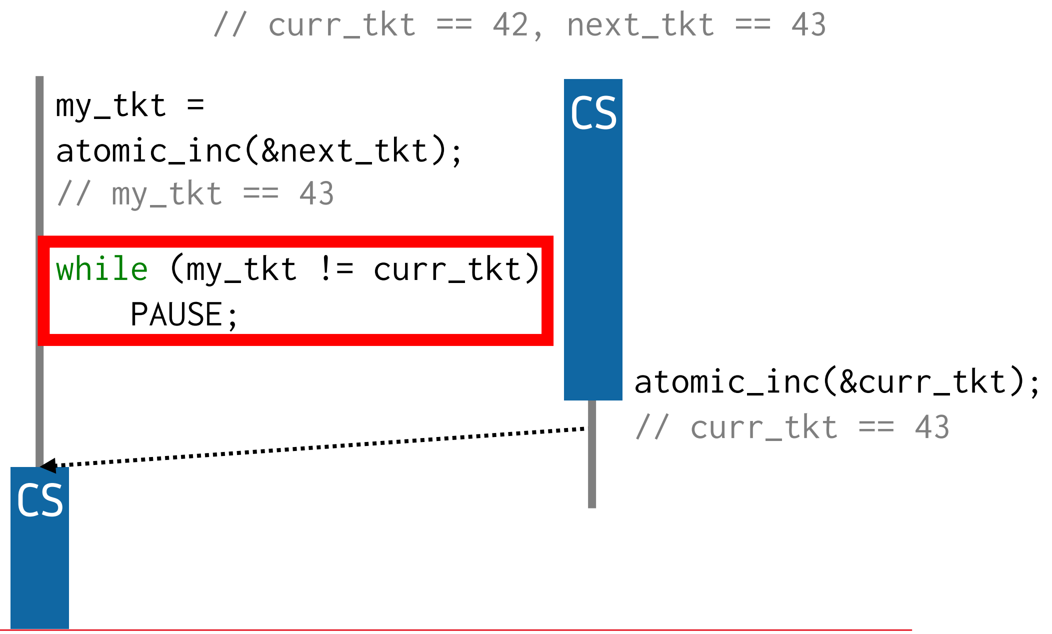

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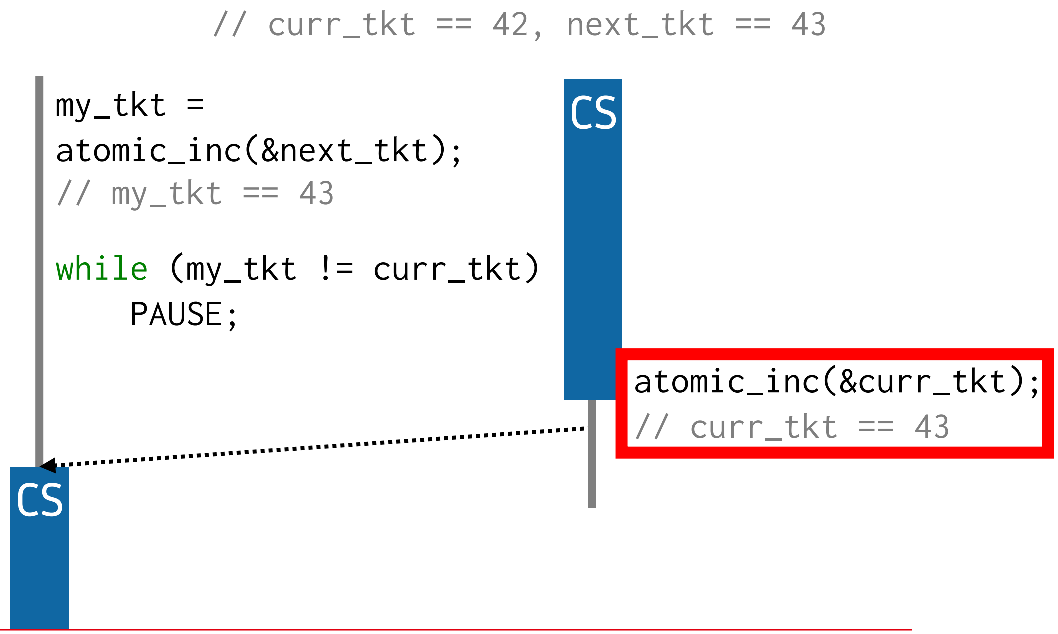
    - **On CS exit:** atomically increment the current ticket



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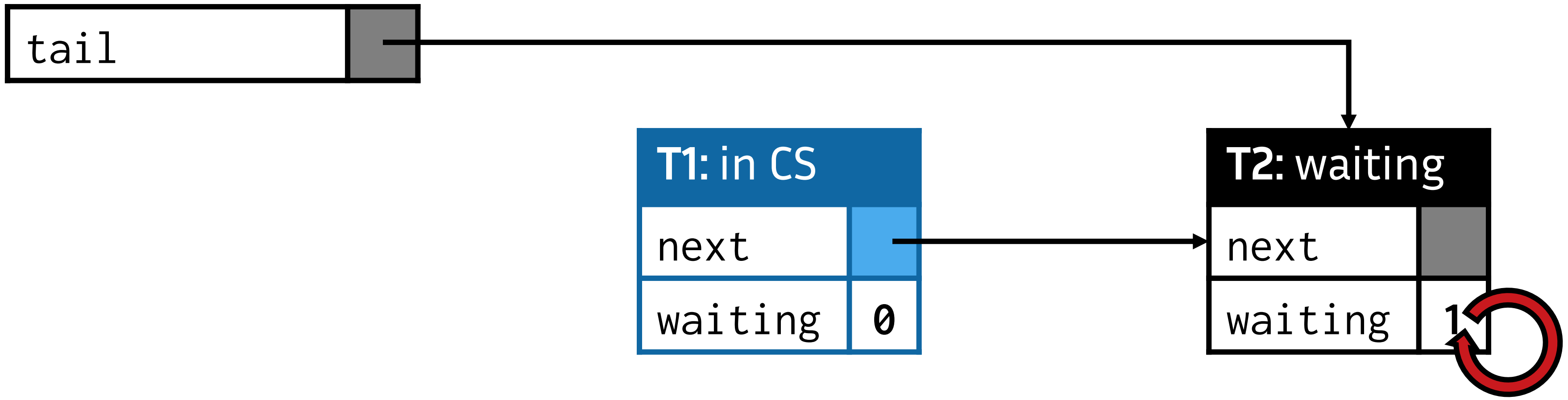

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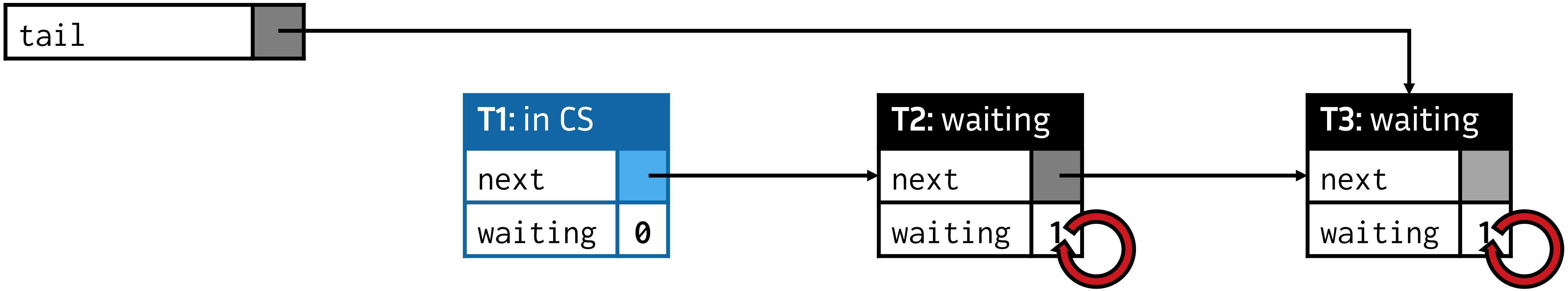

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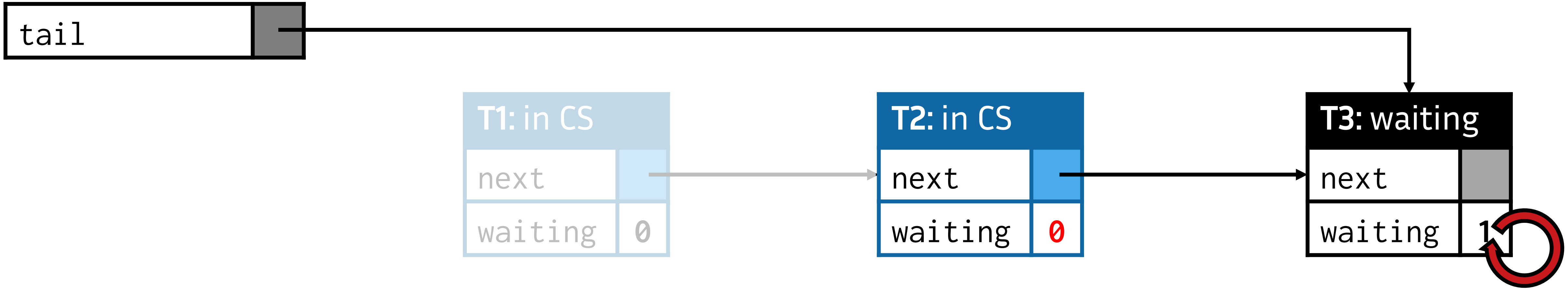

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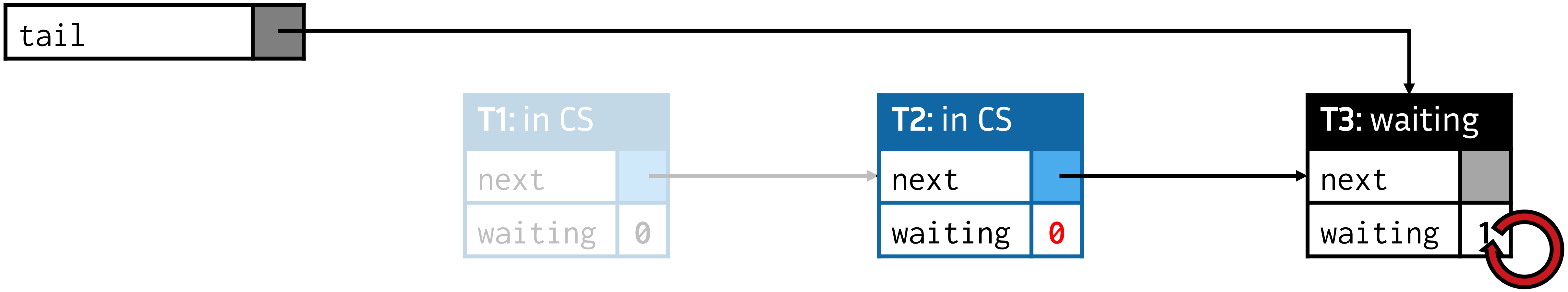
    - **Difference between MCS and CLH:** direction of the queue



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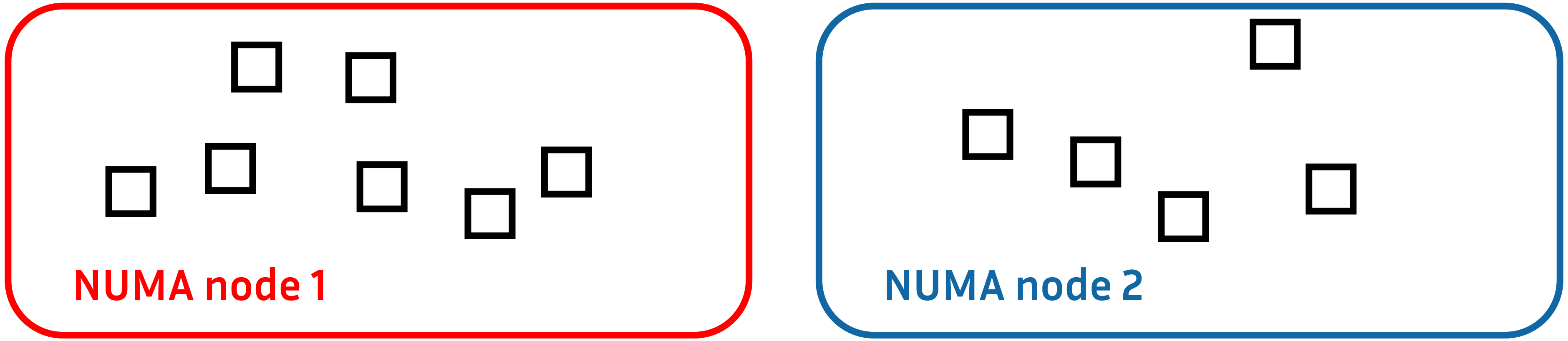

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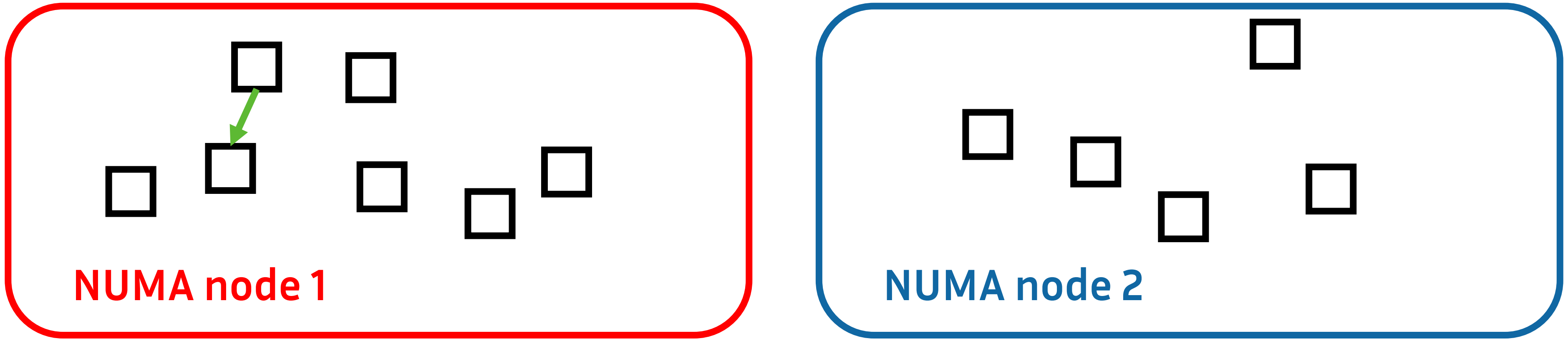

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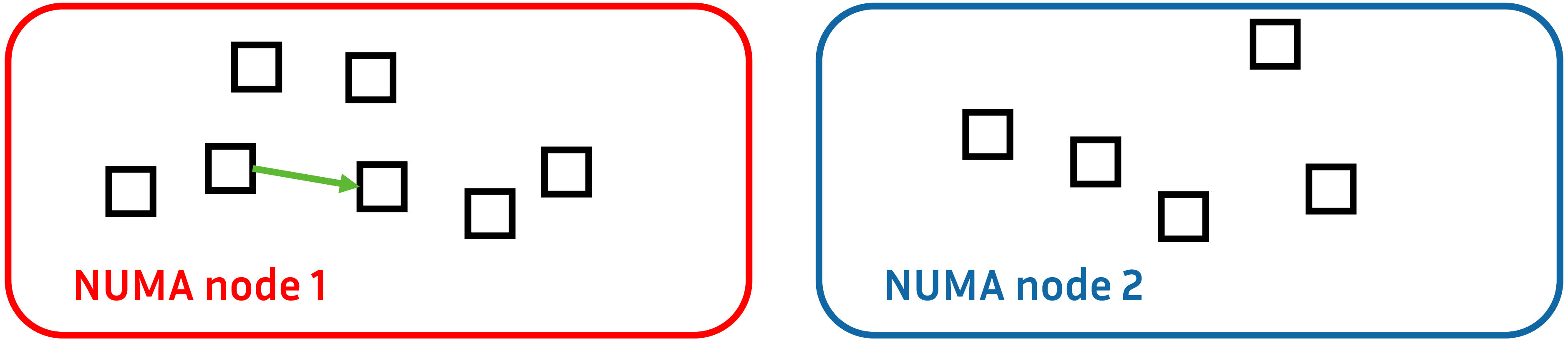

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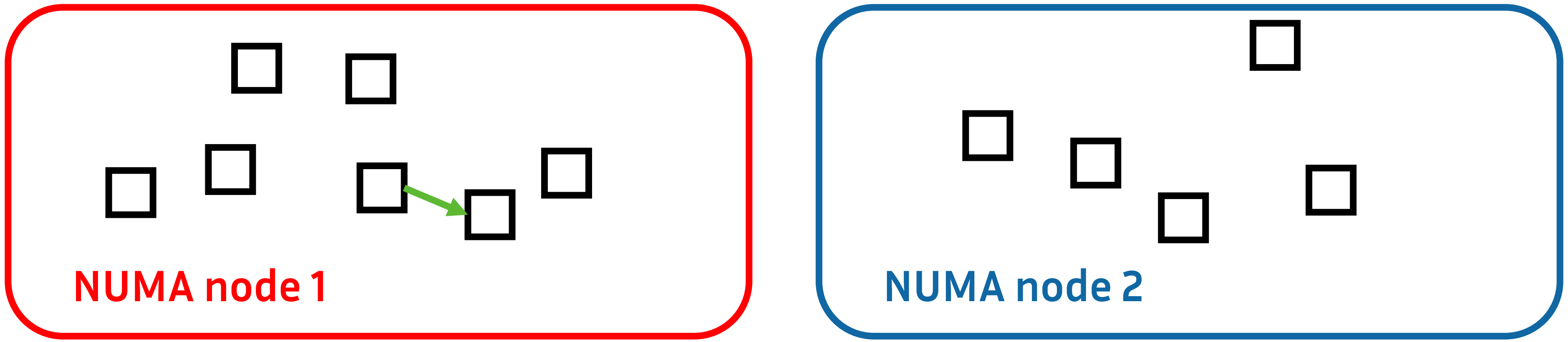

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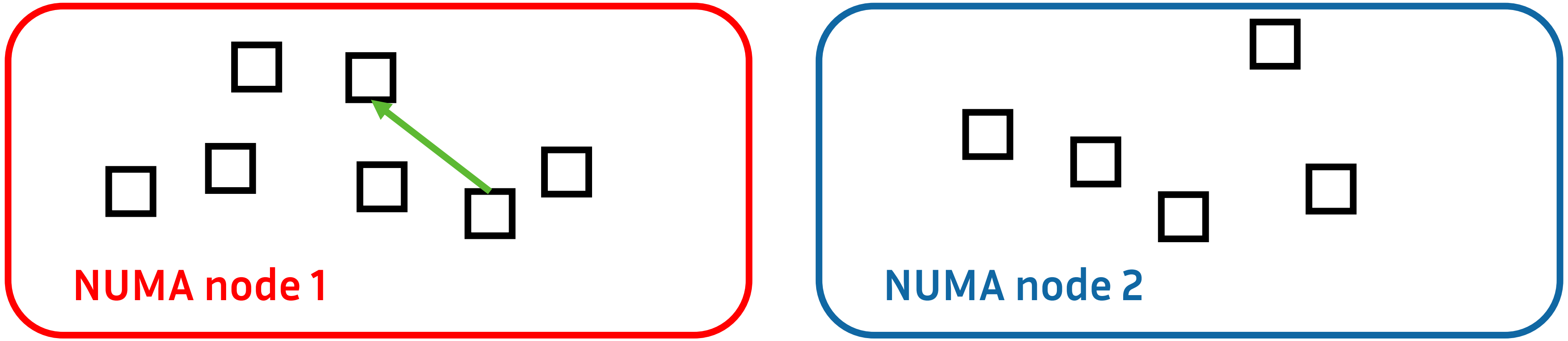

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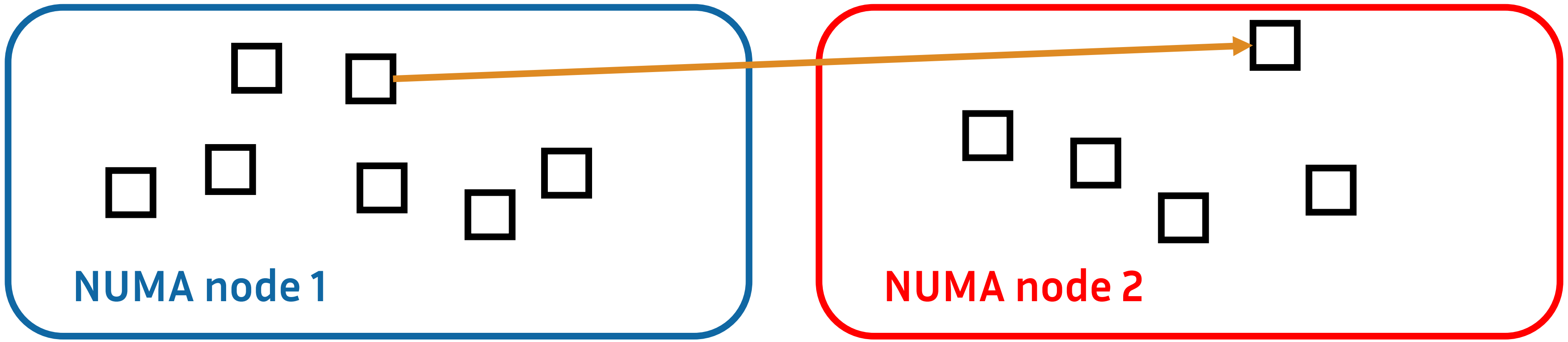

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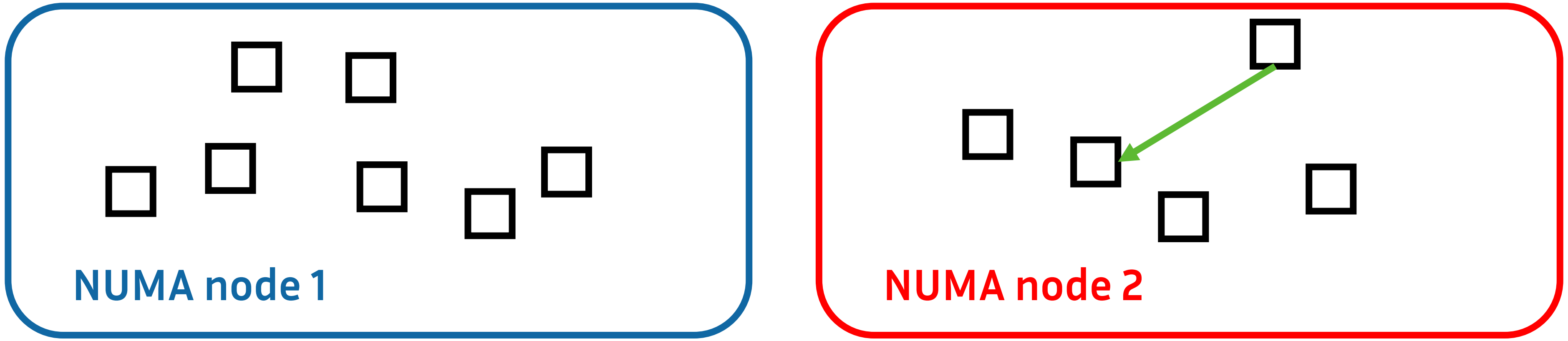

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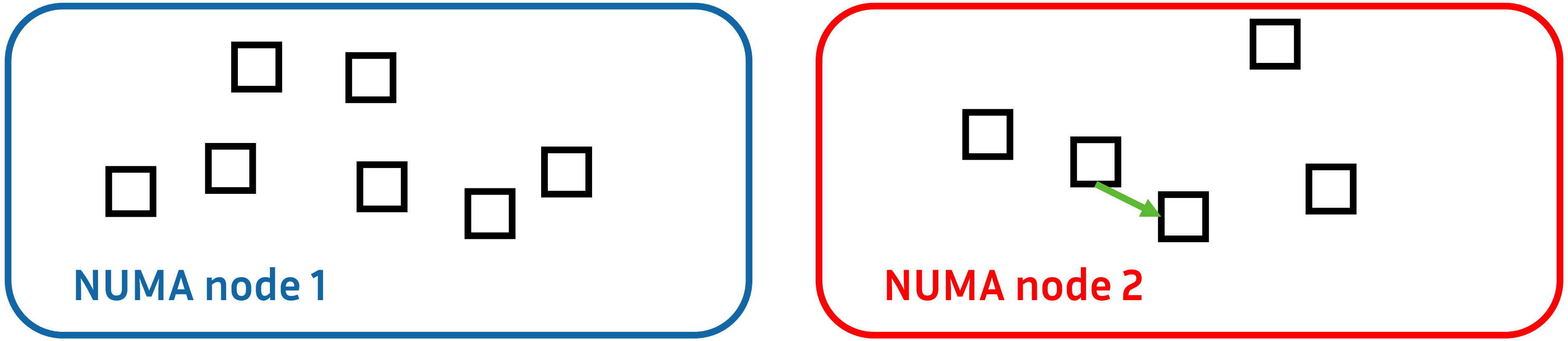

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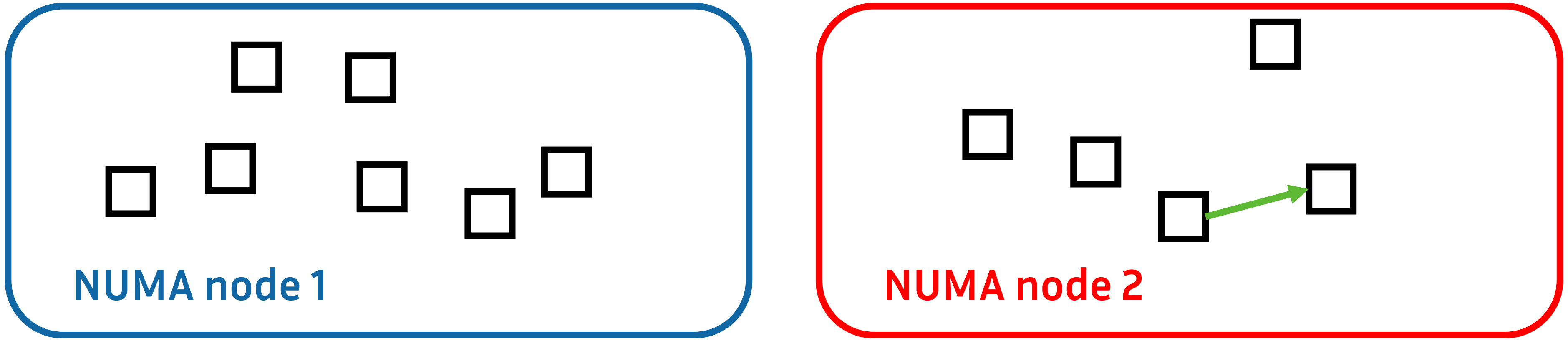

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    if (locked != UNLOCKED)
        mcs_lock(&mcs_lock);
        while (XCHG(&lock, LOCKED) != UNLOCKED)
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    ...
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  - **Advantages:**
    - Fast acquisition when lock free; at most one spinner on the TAS lock
    - At most one MCS acquired at a time, lower memory consumption for nested locks
      - *Only one MCS node per thread needed, instead of one per thread per lock*

```
# Single-variable lock states
# LOCKED_WITH_BLOCKED_WAITERS = at least one thread is blocking,
# the holder should call futex_wake when releasing the lock
UNLOCKED = 0, LOCKED = 1, LOCKED_WITH_BLOCKED_WAITERS = 2
# CS preemption counter updated by the eBPF Preemption Monitor
num_preempted_cs = 0

class Lock:
  val = UNLOCKED, queue = None # Single-variable lock, MCS tail
class QNode:
  next = None, waiting = False

def mcs_exit(lock: Lock, qnode: QNode):
  if qnode.next is None:
    if CAS(&lock.queue, qnode, None) == qnode:
      return
    while qnode.next is None:
      PAUSE()
  qnode.next.waiting = False

def flexguard_unlock(lock: Lock, qnode: QNode):
  qnode.cs_counter -= 1
label at_unlock
  if XCHG(&lock.val, UNLOCKED) == LOCKED_WITH_BLOCKED_WAITERS:
    futex_wake(&lock.val, 1) # Wake one of the waiting threads

def flexguard_lock(lock: Lock, qnode: QNode):
label at_fastpath # Try to steal the single-variable lock if free
  if lock.val == UNLOCKED and CAS(&lock.val, UNLOCKED, LOCKED):
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  # There are waiters in the queue, enter the slow path
  flexguard_slow_path(lock, qnode)
```

```
def flexguard_slow_path(lock, qnode):
  enqueued = False
  if num_preempted_cs == 0: # If spinning, begin Phase 1
    enqueued = True
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    qnode.waiting = True
label at_xchg
    pred = XCHG(&lock.queue, qnode)
    if pred is not None:
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      while qnode.waiting and num_preempted_cs == 0:
        PAUSE()
label at_phase2 # Begin Phase 2
  state = CAS(&lock.val, UNLOCKED, LOCKED)
  while state != UNLOCKED:
    if num_preempted_cs == 0: # Busy-waiting mode
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          return flexguard_slow_path(lock, qnode)
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FlexGuard’s lock algorithm

- Similar TAS+MCS optimization as the **Shuffle lock**
  - But the TAS lock variable can also be used as the FUTEX lock variable

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      while qnode.waiting and num_preempted_cs == 0:
        PAUSE()
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⇒ Possible to acquire the lock as spinning or blocking

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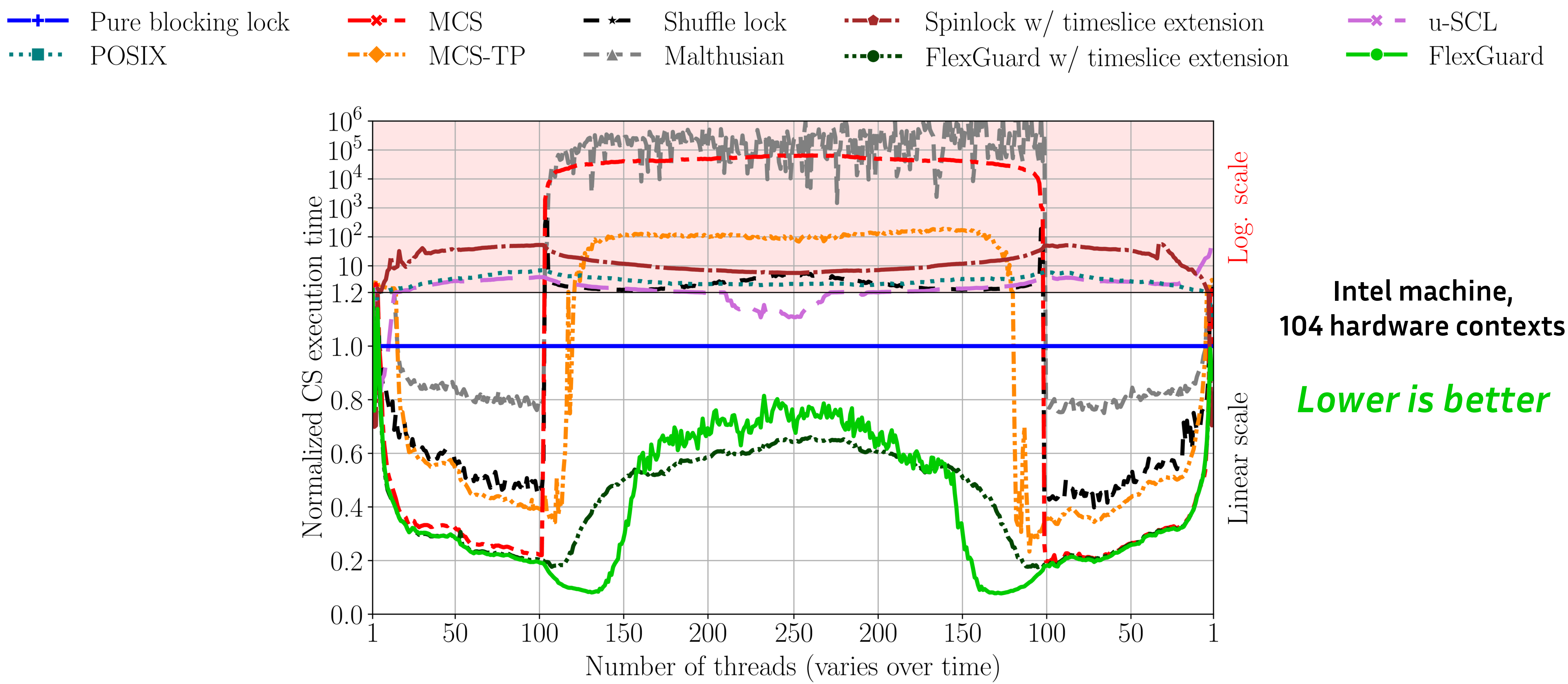
- **In blocking mode:** MCS queue bypassed!

- **Spinning→blocking transition:** spin waiters exit the MCS queue
- **Blocking→spinning transition:** blocking waiters reenqueue themselves in the MCS queue
  - *One woken up at each `unlock()` if there are blocked waiters, TAS attempt then reenqueuing*

Evaluation: microbenchmark (Intel)

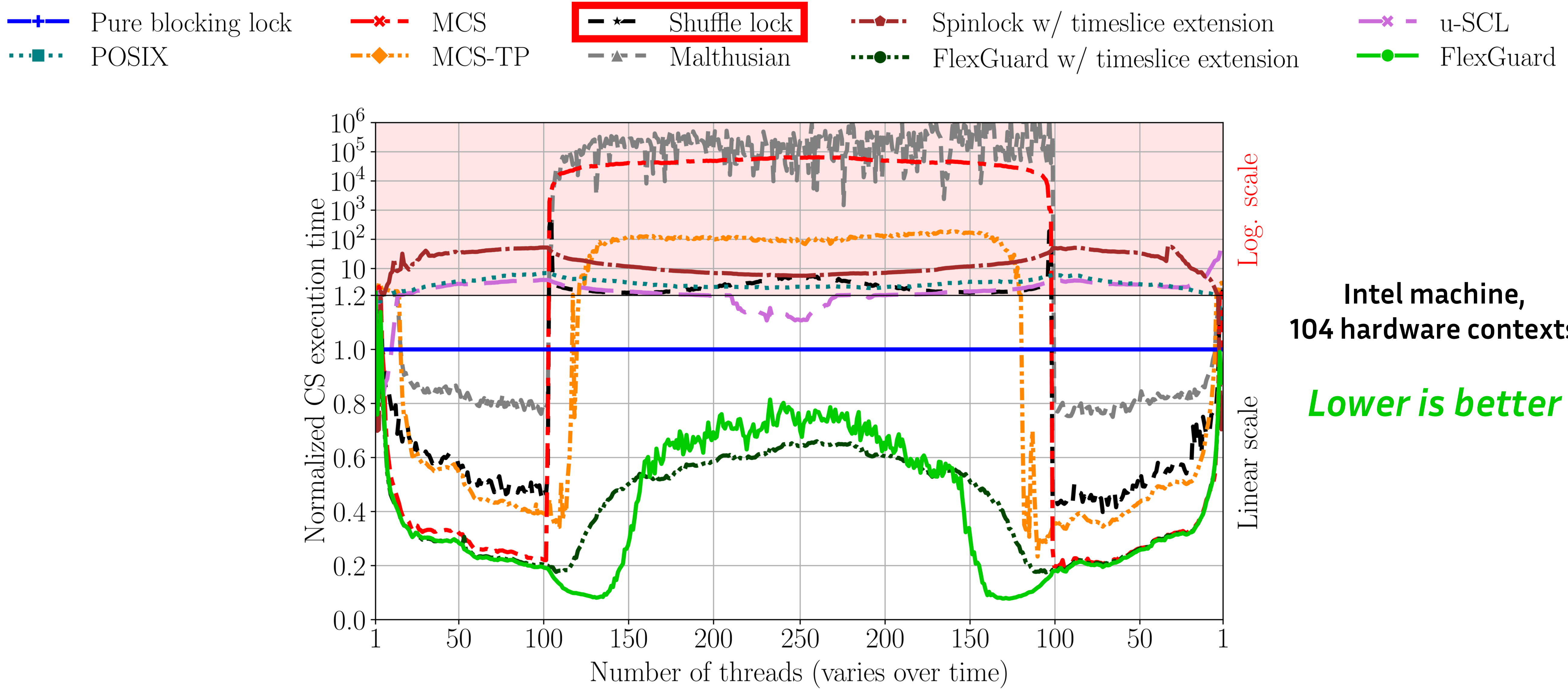


Intel machine,
104 hardware contexts

Lower is better

Evaluation: microbenchmark (Intel)

With spin-then-park

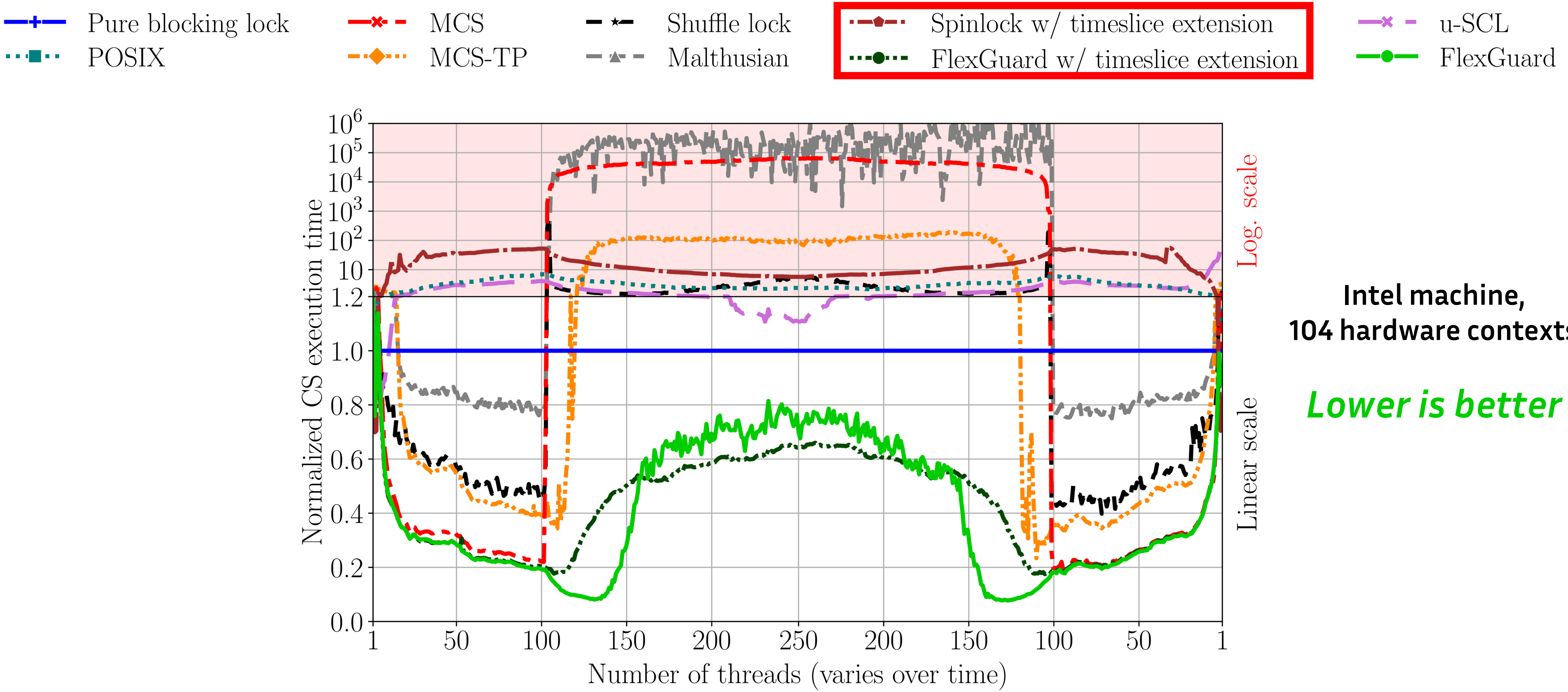


Intel machine, 104 hardware contexts

Lower is better

Evaluation: microbenchmark (Intel)

Recently proposed patch for Linux
Applicable to our approach



Intel machine,
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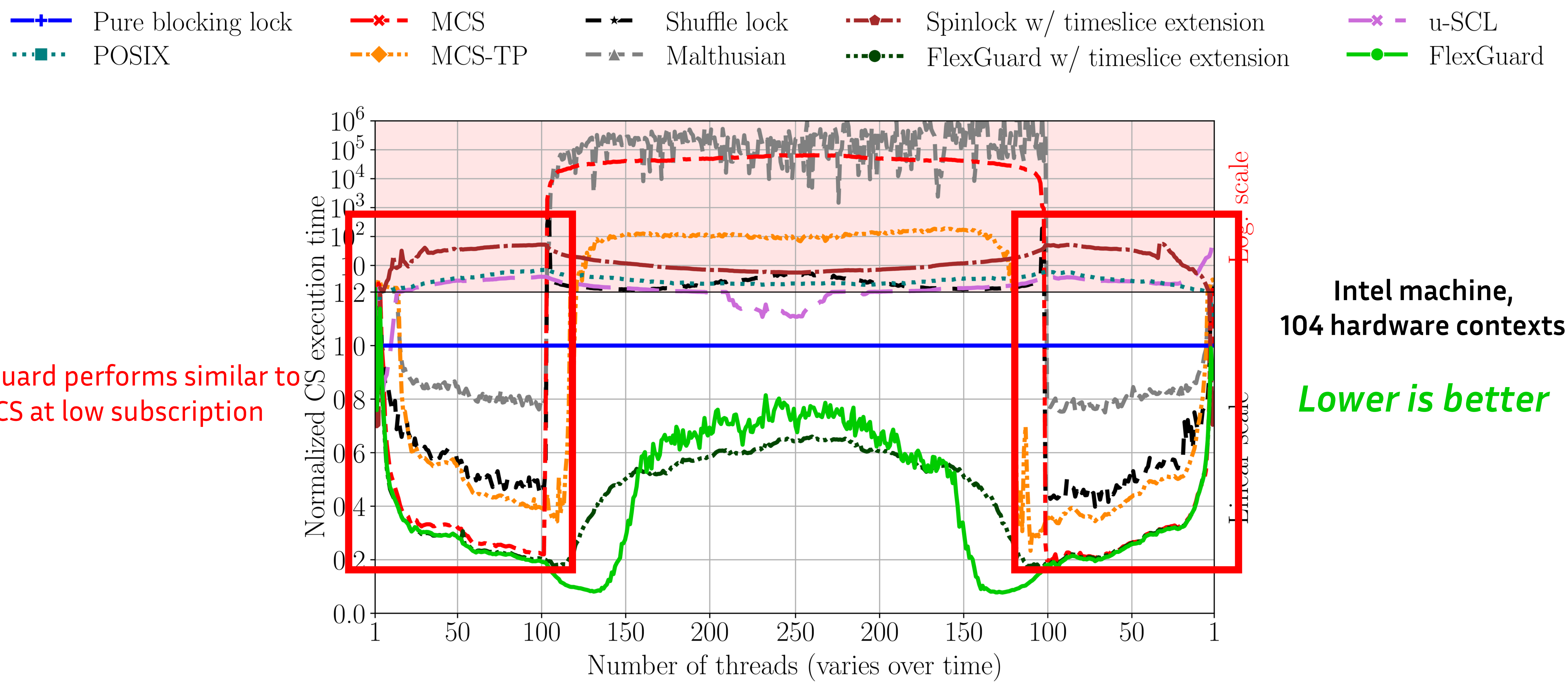

FlexGuard performs similar to MCS at low subscription

Intel machine,
104 hardware contexts

Lower is better

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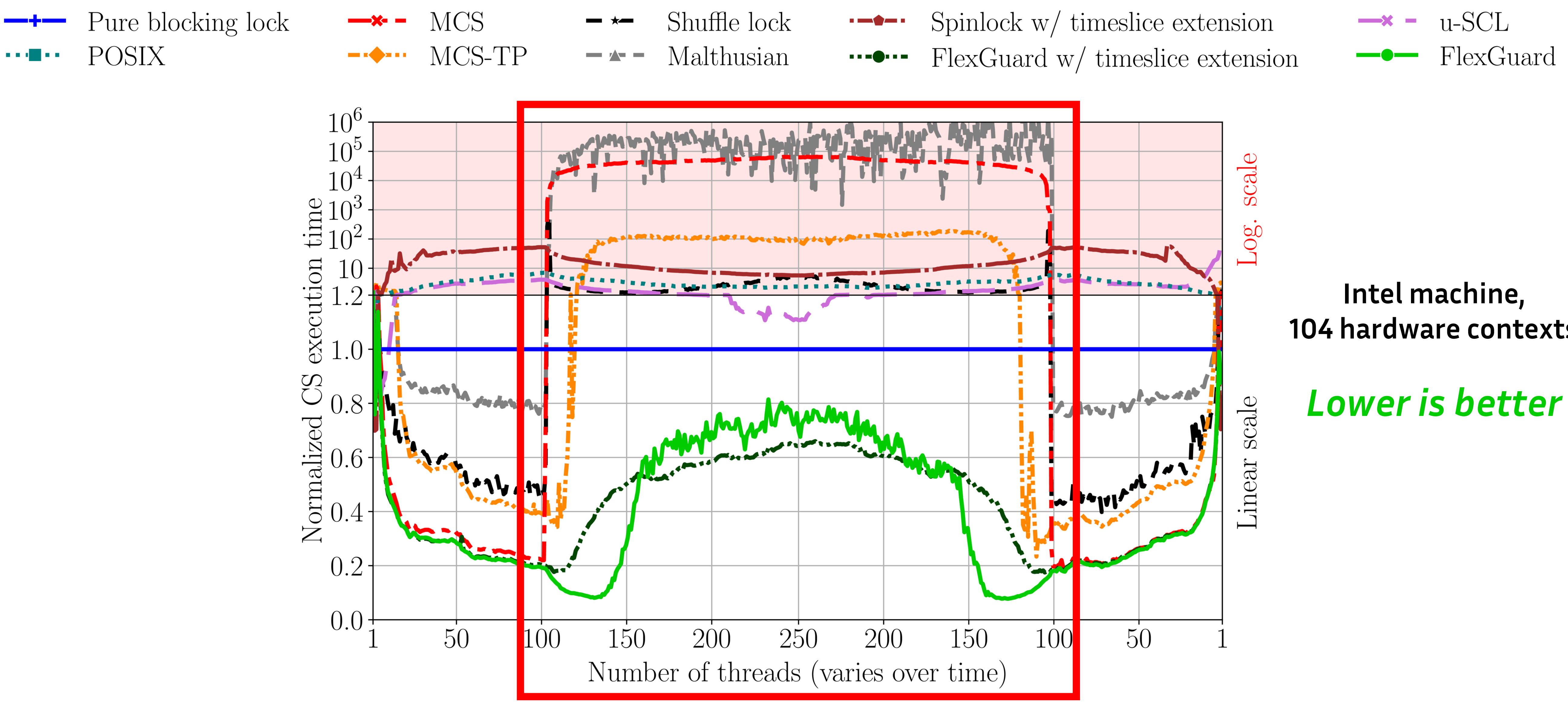


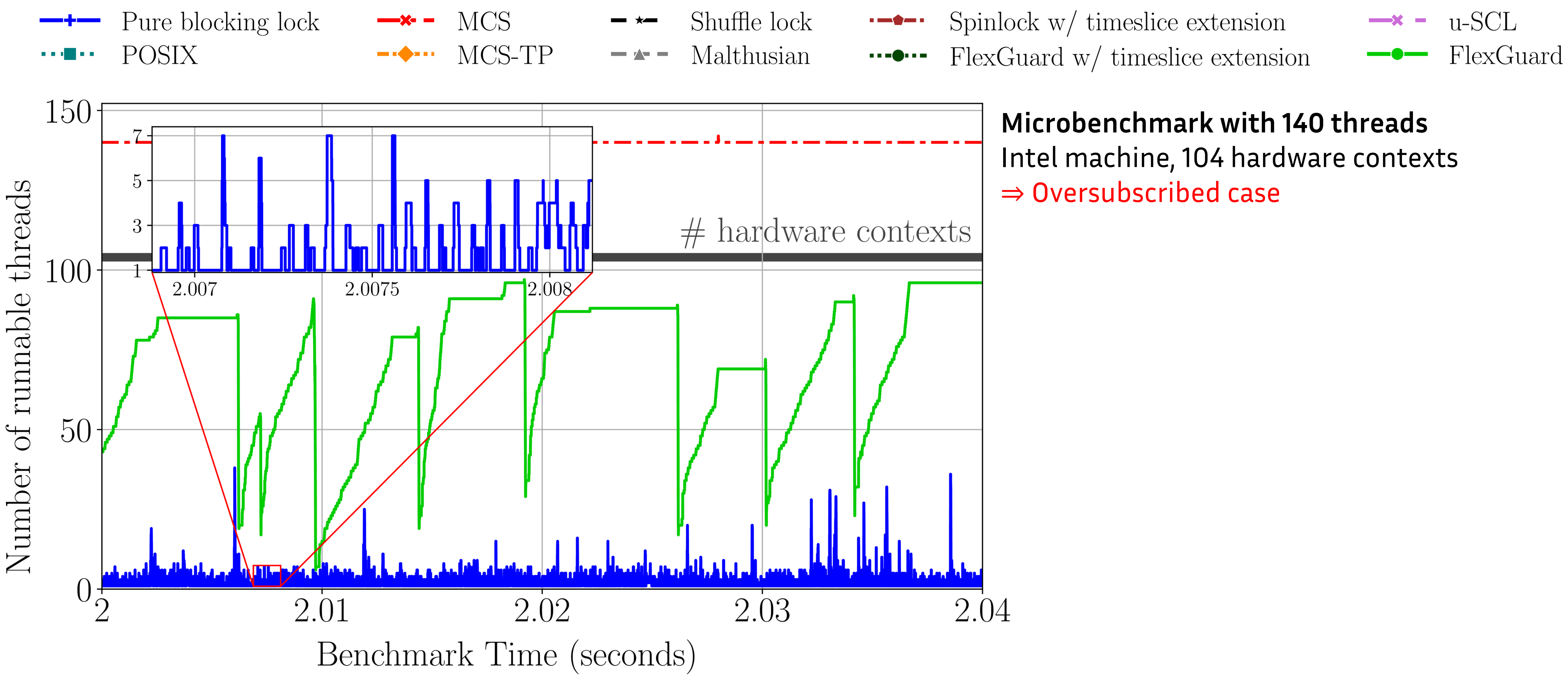
Intel machine, 104 hardware contexts

Lower is better

FlexGuard avoids the performance collapse at high subscription

Even greatly outperforms the blocking locks… but why?

Runnable threads

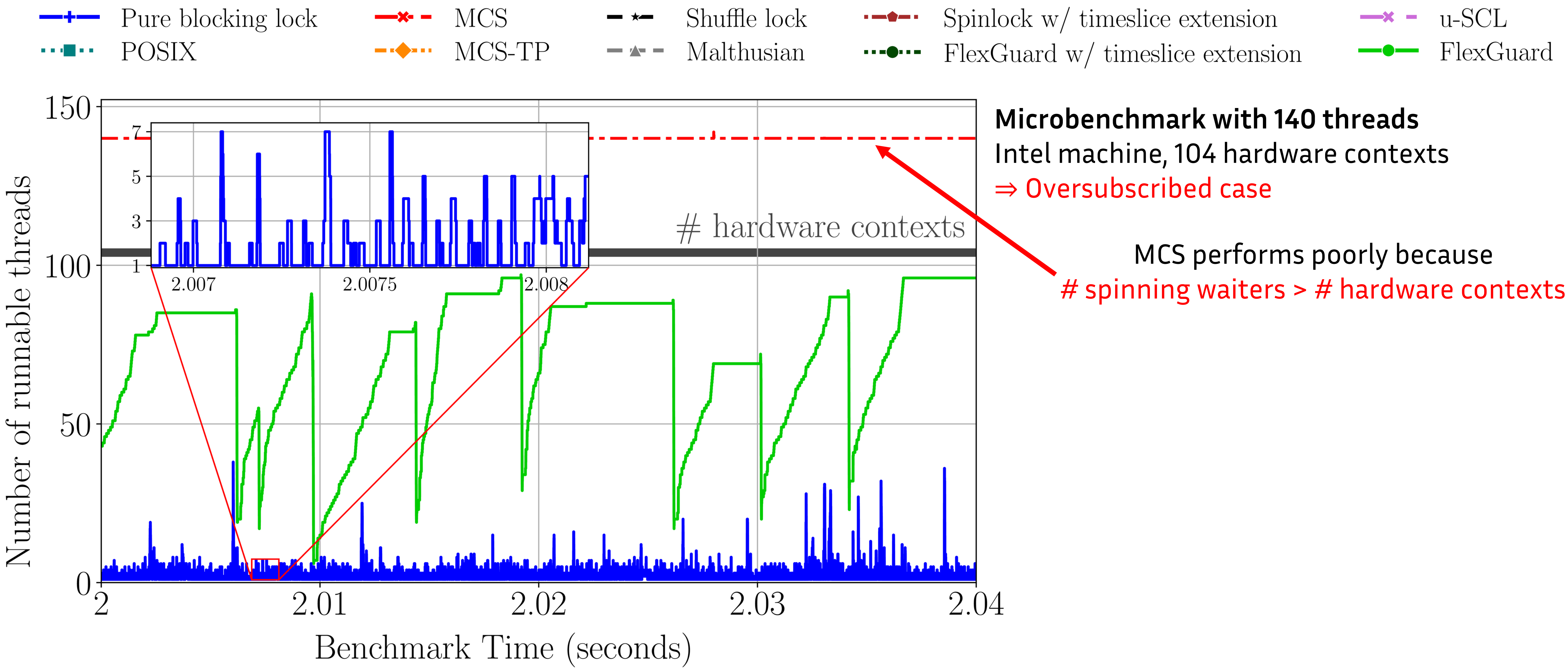


Microbenchmark with 140 threads

Intel machine, 104 hardware contexts

⇒ Oversubscribed case

Runnable threads



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Intel machine, 104 hardware contexts

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MCS performs poorly because

spinning waiters > # hardware contexts

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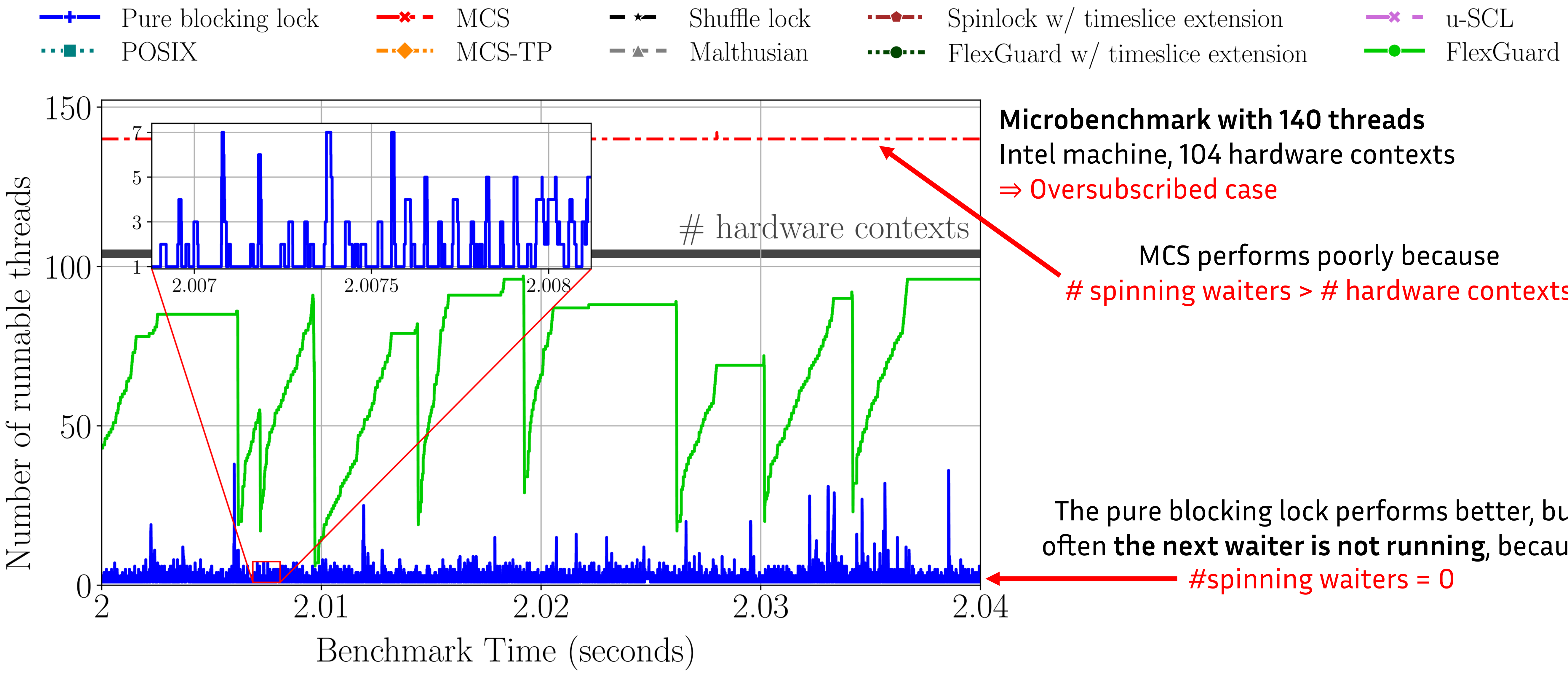

Microbenchmark with 140 threads

Intel machine, 104 hardware contexts

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The pure blocking lock performs better, but often **the next waiter is not running**, because

#spinning waiters = 0

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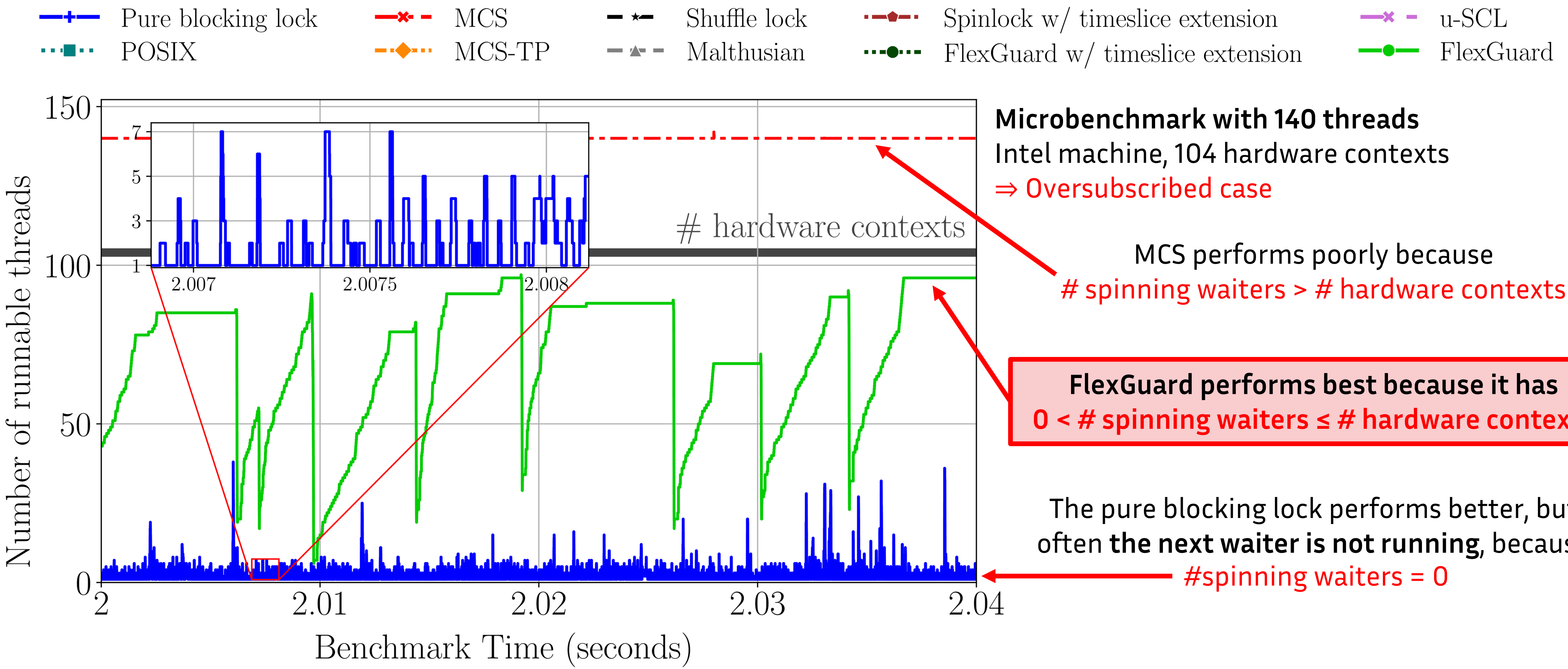

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Intel machine, 104 hardware contexts
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FlexGuard performs best because it has
0 < # spinning waiters ≤ # hardware contexts

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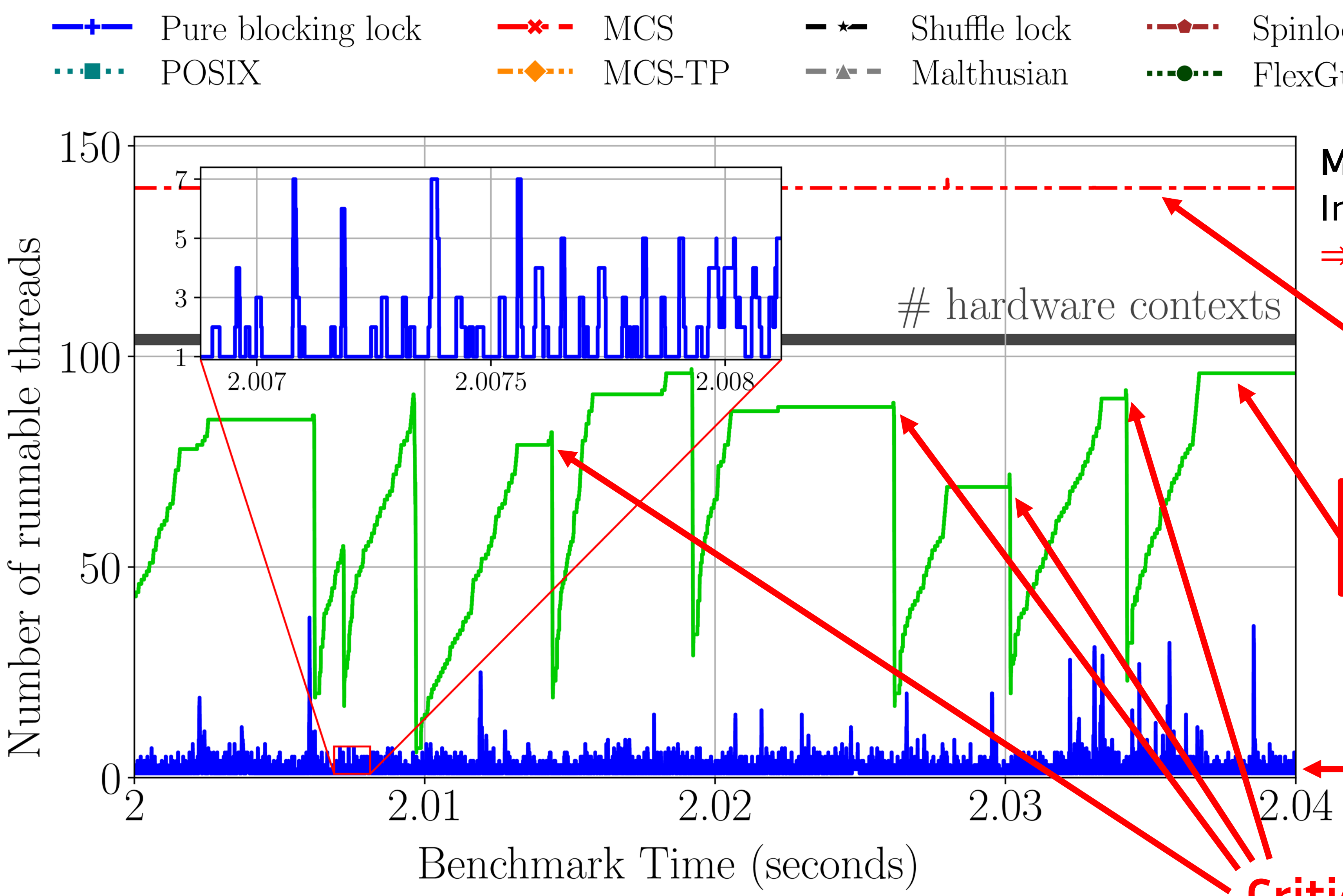

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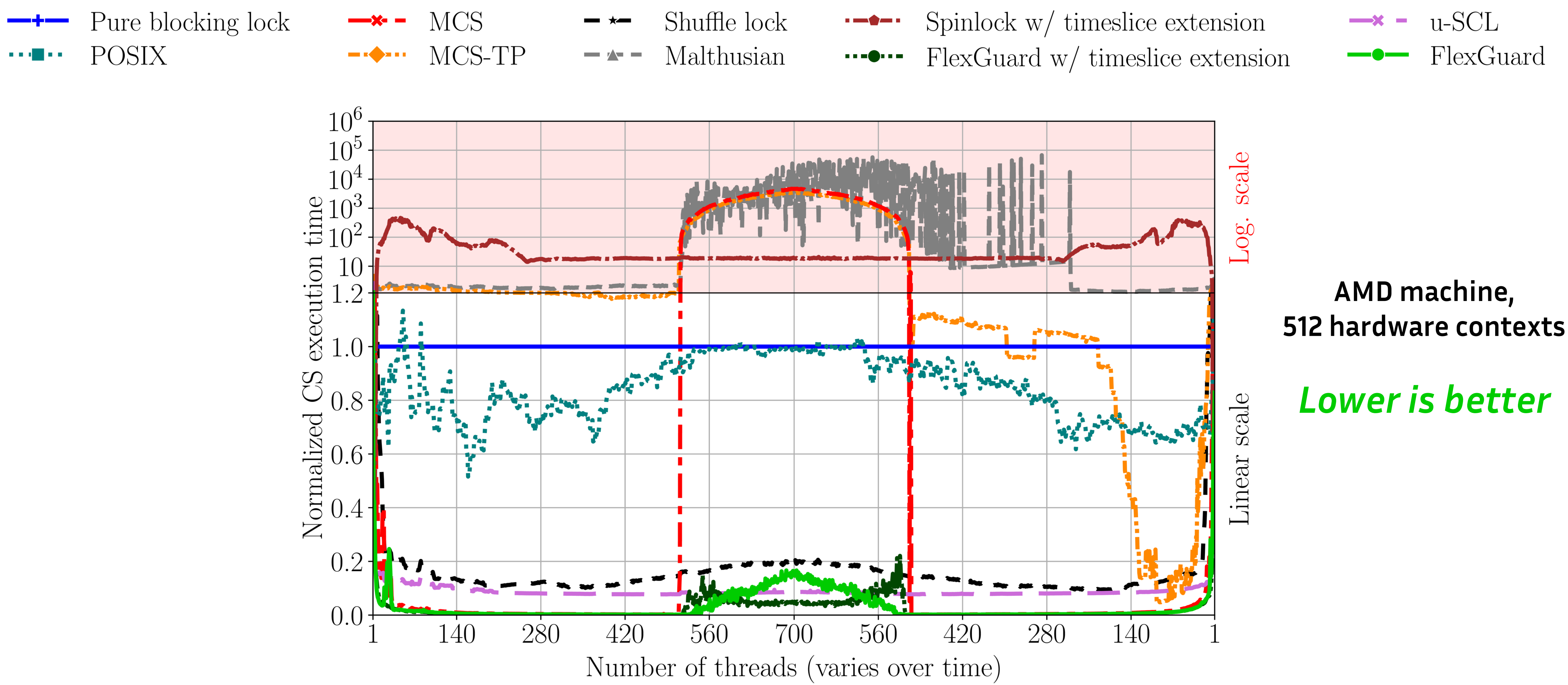
Critical section preemptions

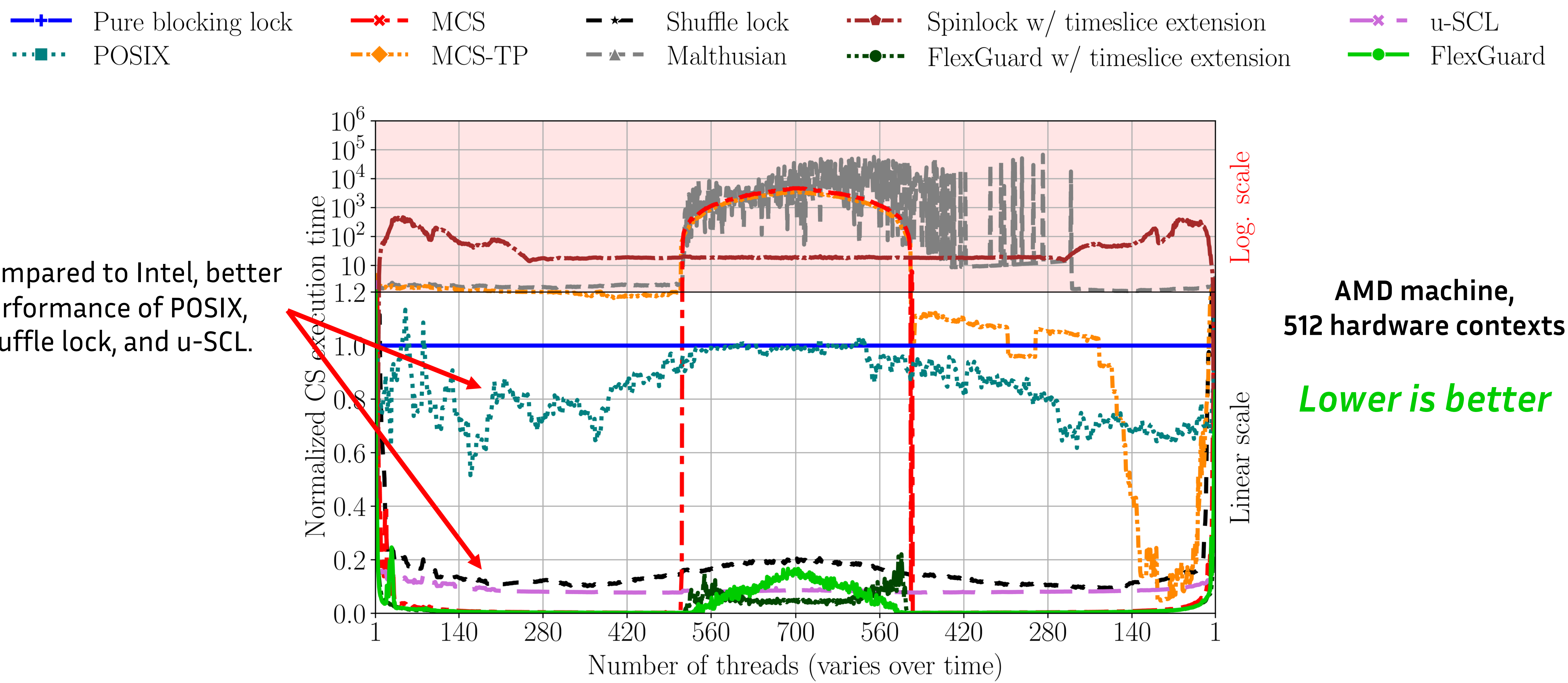
Evaluation: microbenchmark (AMD)



AMD machine, 512 hardware contexts

Lower is better

Evaluation: microbenchmark (AMD)

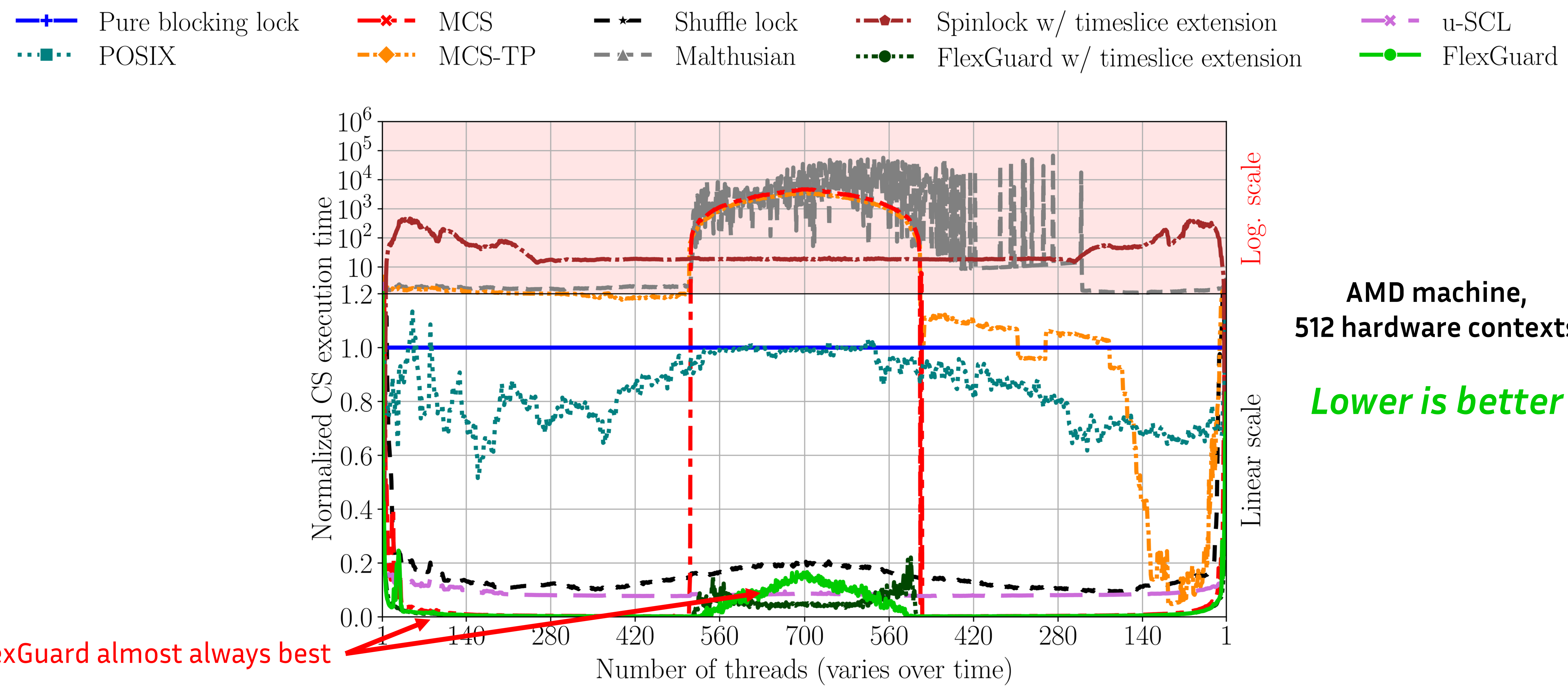


As compared to Intel, better performance of POSIX, Shuffle lock, and u-SCL.

AMD machine, 512 hardware contexts

Lower is better

Evaluation: microbenchmark (AMD)

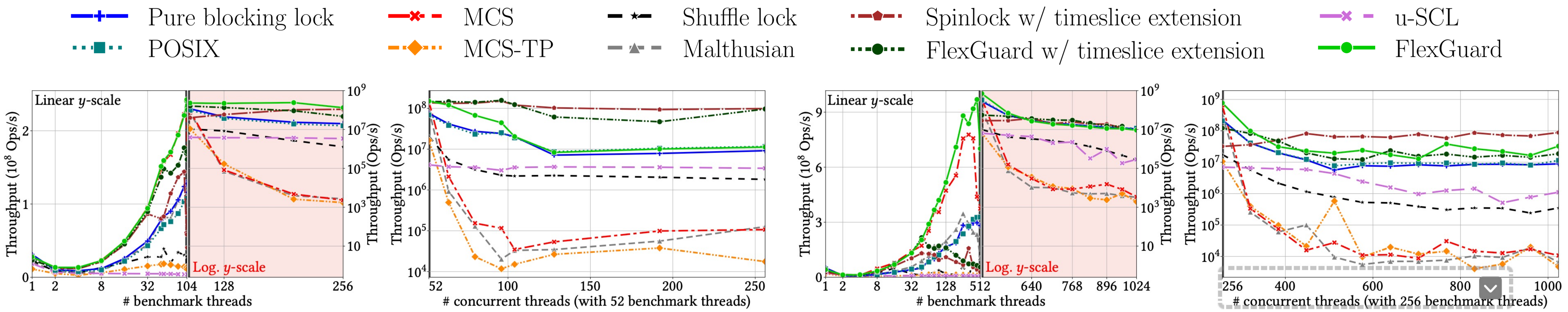


FlexGuard almost always best

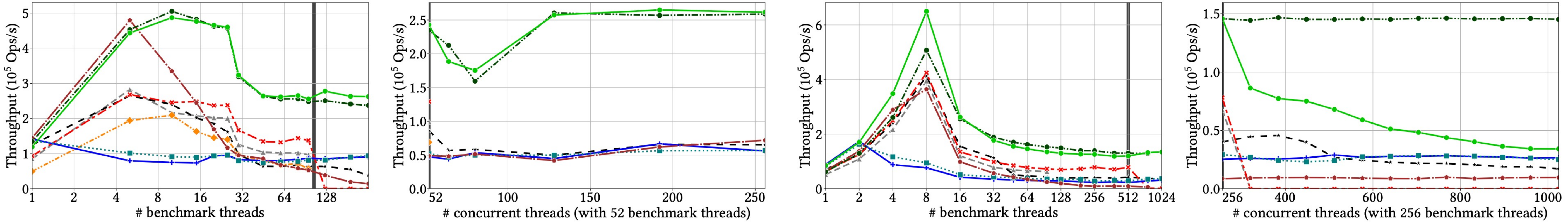
AMD machine,
512 hardware contexts

Lower is better

Evaluation: benchmarks



(a) Hash table on Intel. **(b)** Hash table on Intel w/ conc. **(c)** Hash table on AMD. **(d)** Hash table on AMD w/ conc.

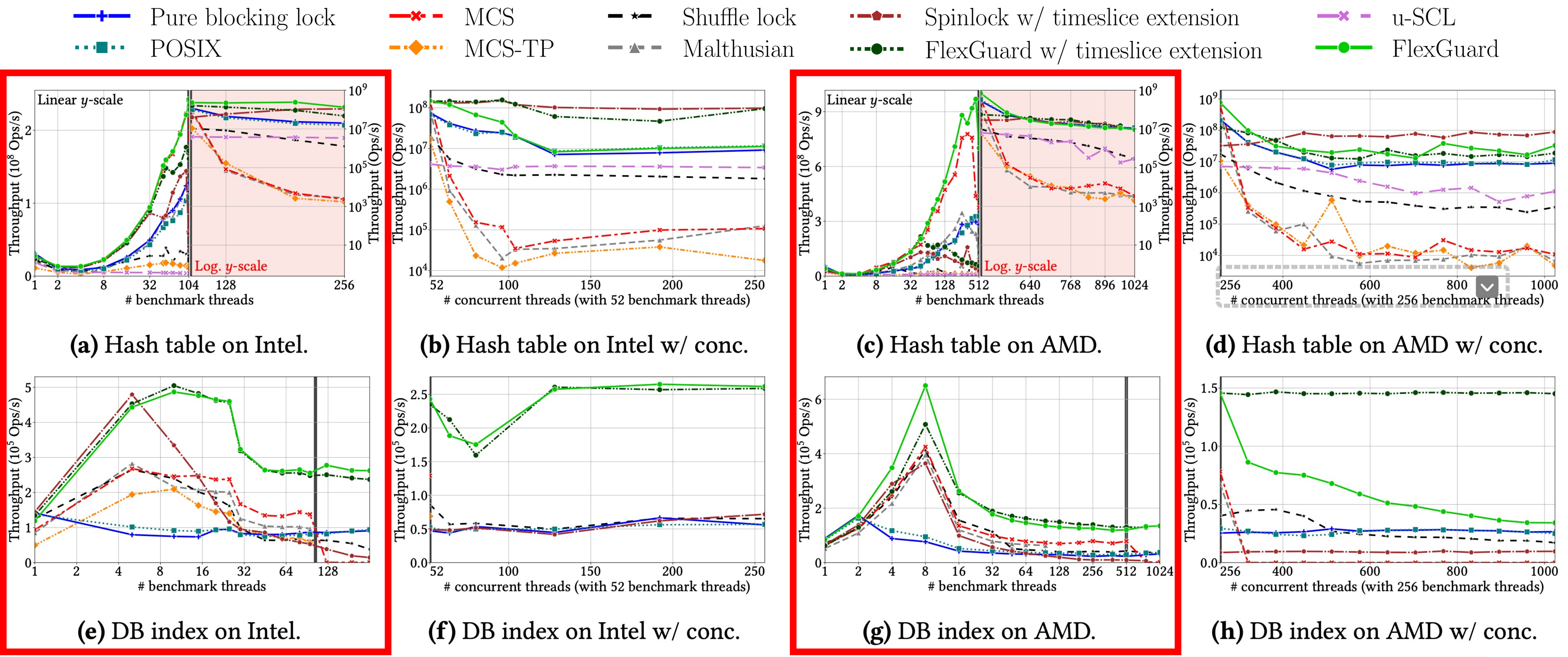


(e) DB index on Intel. **(f)** DB index on Intel w/ conc. **(g)** DB index on AMD. **(h)** DB index on AMD w/ conc.

Higher is better

Evaluation: benchmarks

FlexGuard matches or outperforms other locks on both low and high subscription



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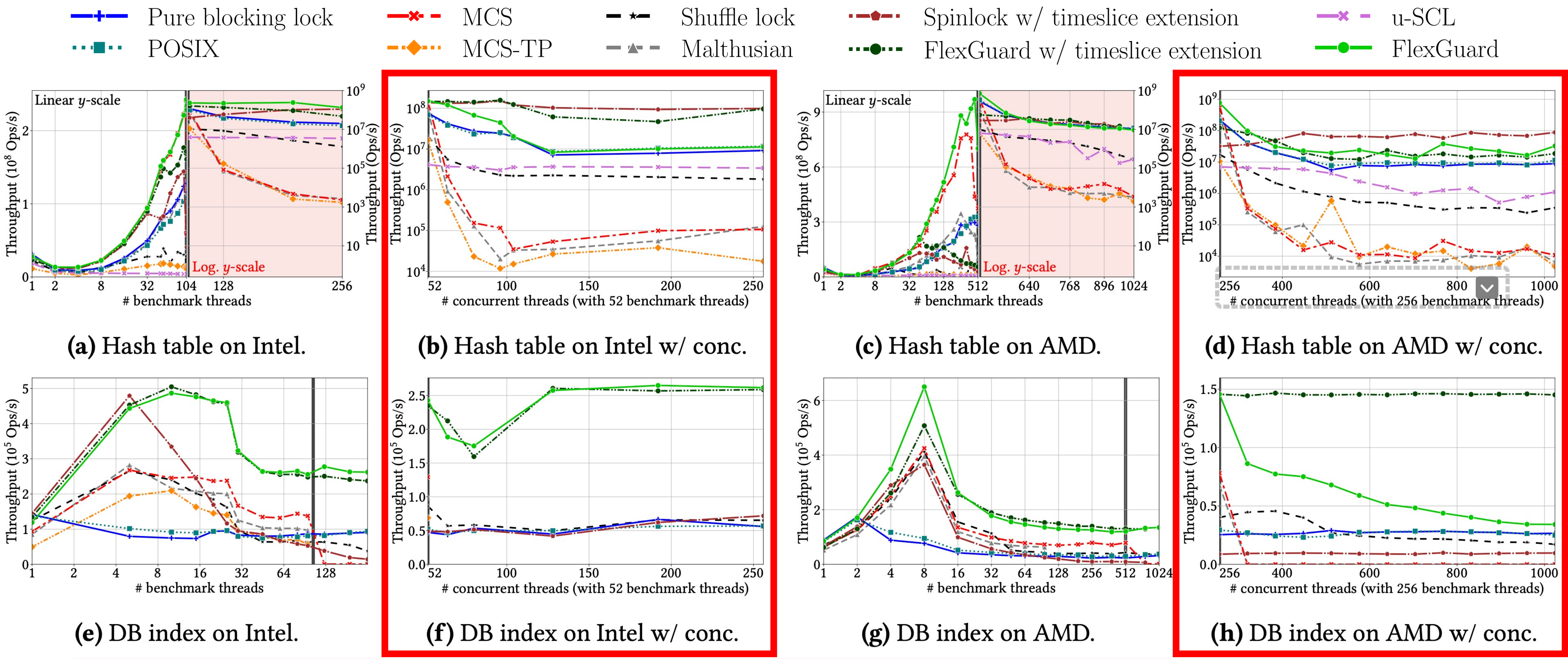
Evaluation: benchmarks

Benchmarks w/ concurrent workload: fixed number of benchmark threads, varying number of concurrent threads

In this case, timeslice extension helps because the concurrent workload's threads cannot be blocked



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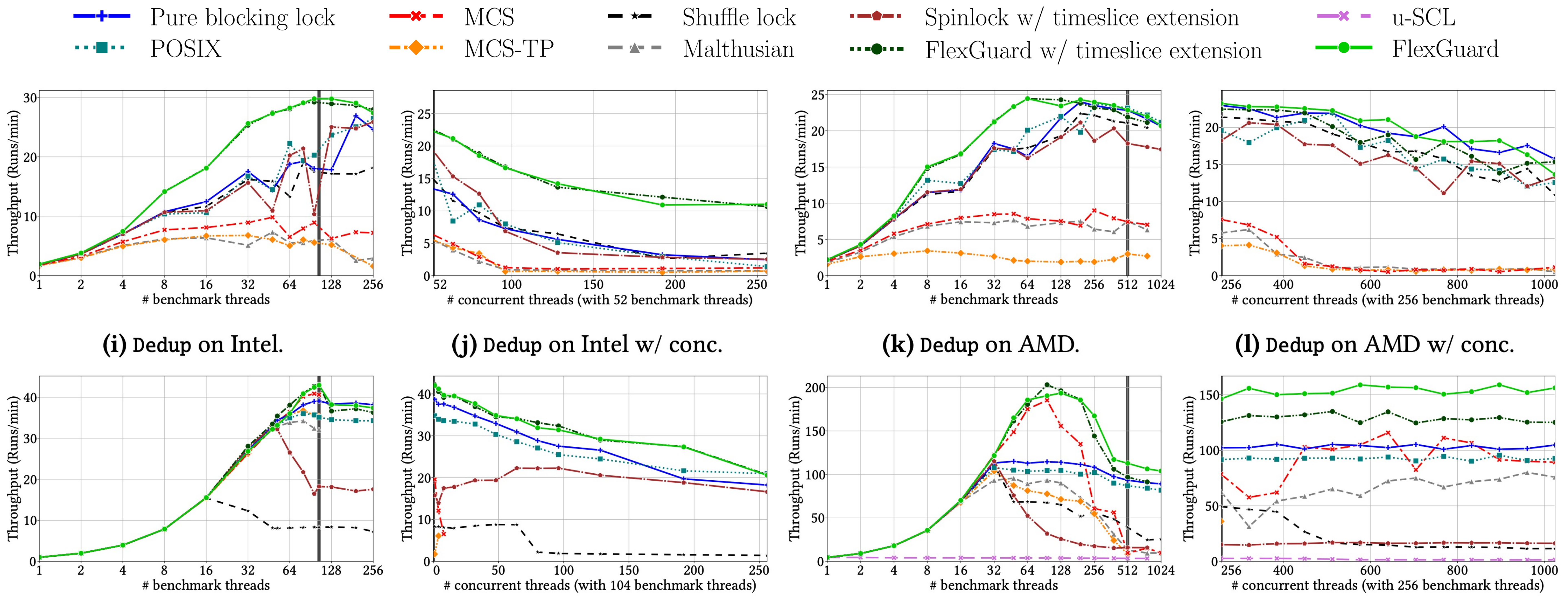

(i) Dedup on Intel.

(j) Dedup on Intel w/ conc.

(k) Dedup on AMD.

(l) Dedup on AMD w/ conc.

(m) Raytrace on Intel.

(n) Raytrace on Intel w/ conc.

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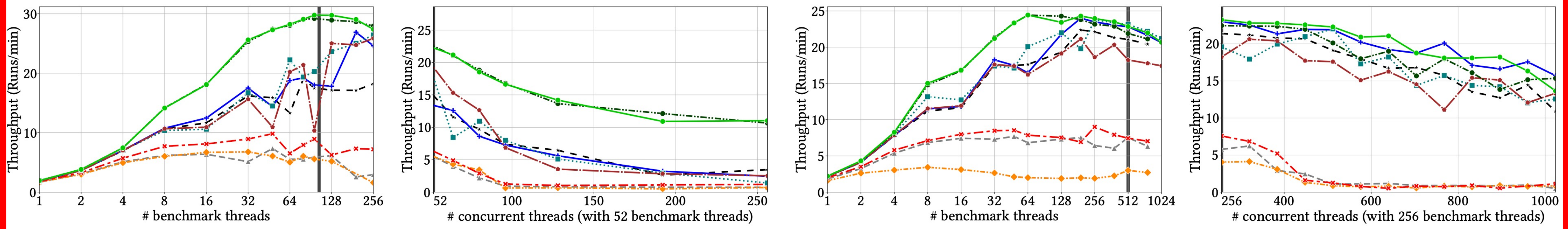
Higher is better

Evaluation: benchmarks

Poor performance of MCS, MCS-TP, and Malthusian, due to the high number of locks (266K): one queue node per thread **and per lock**, many cache misses

FlexGuard performs well due to the Shuffle lock optimization

Pure blocking lock · MCS · Shuffle lock · Spinlock w/ timeslice extension · u-SCL
POSIX · MCS-TP · Malthusian · FlexGuard w/ timeslice extension · FlexGuard



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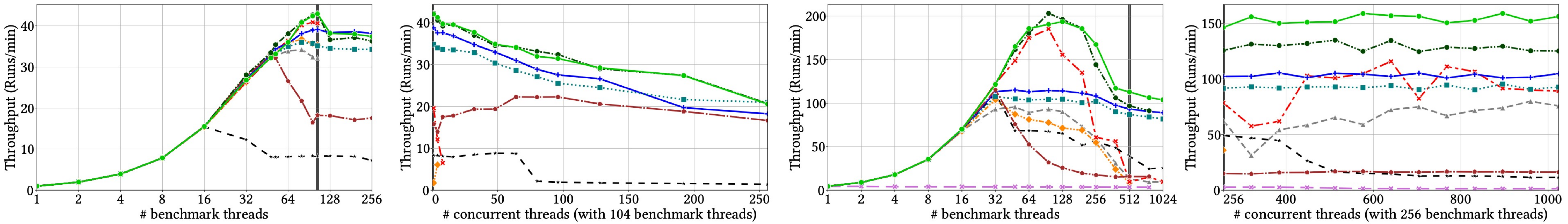

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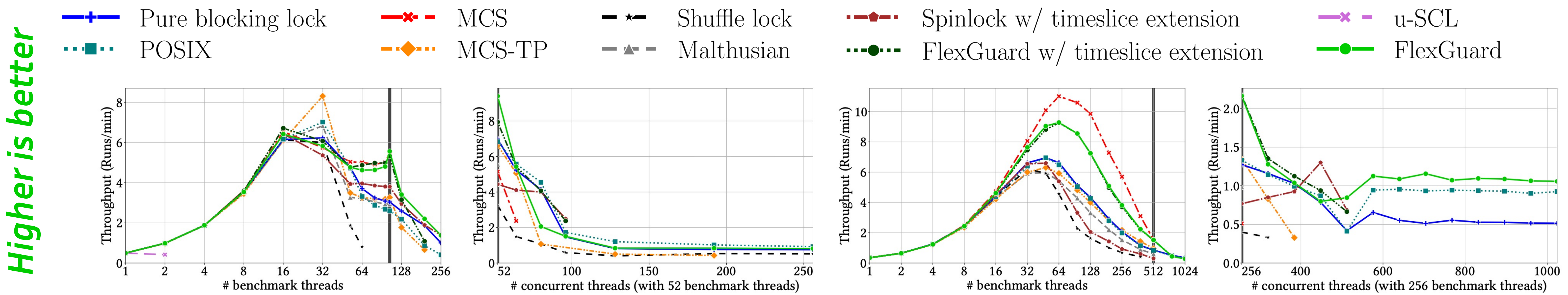

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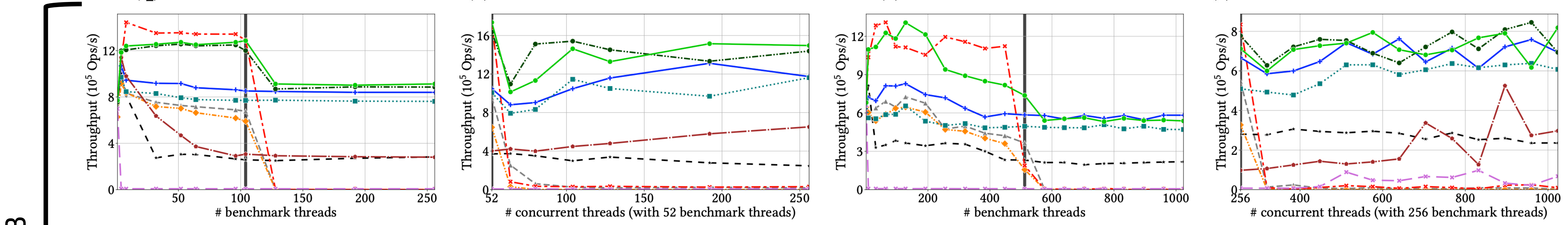

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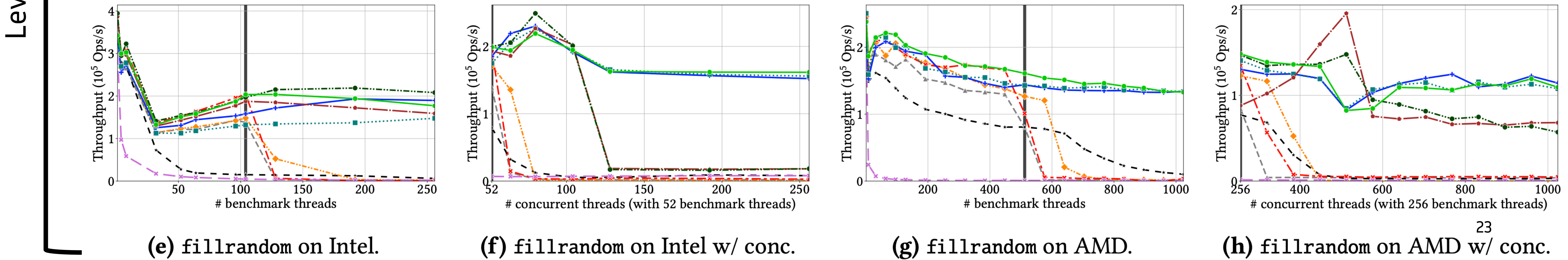

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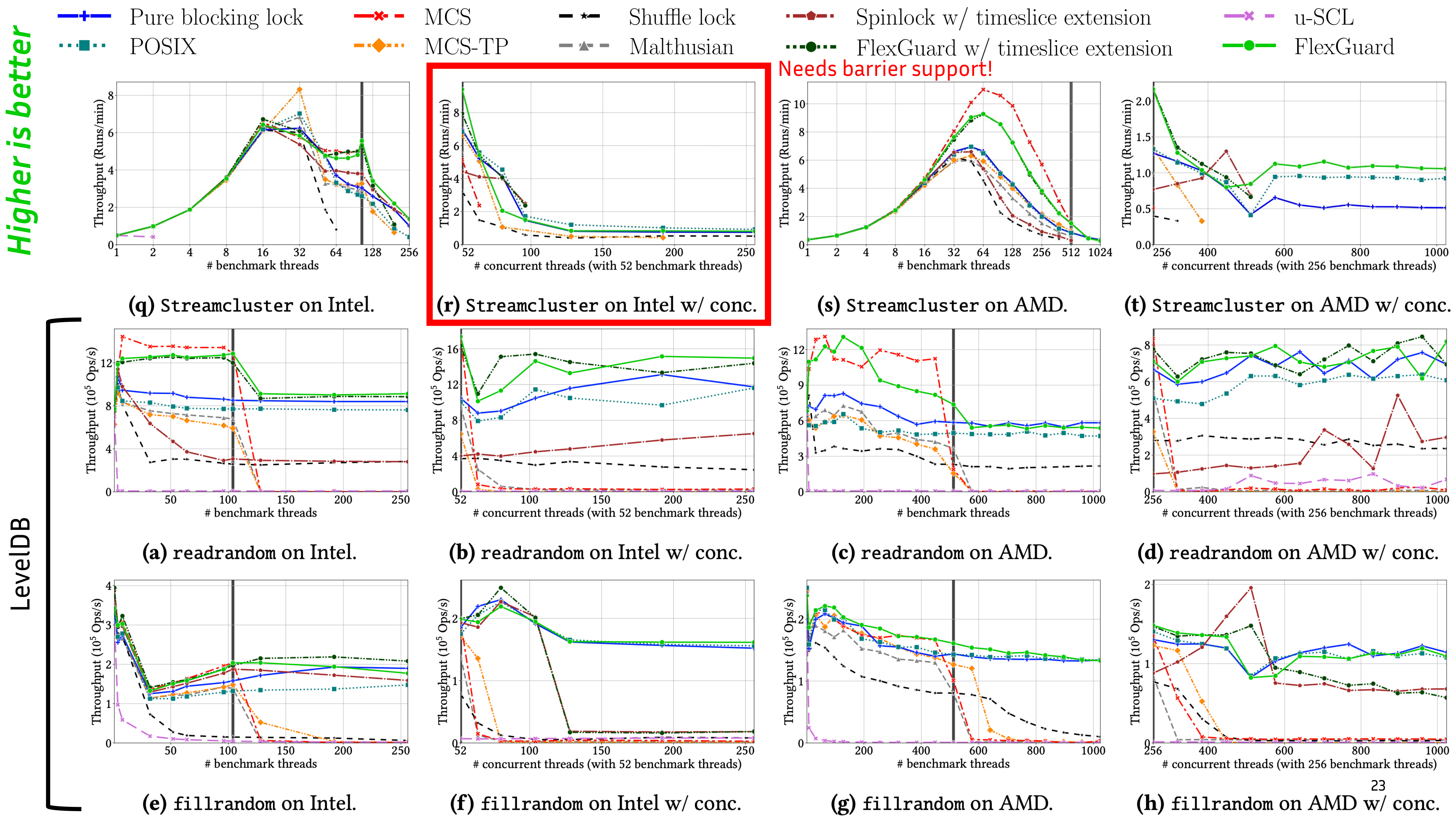

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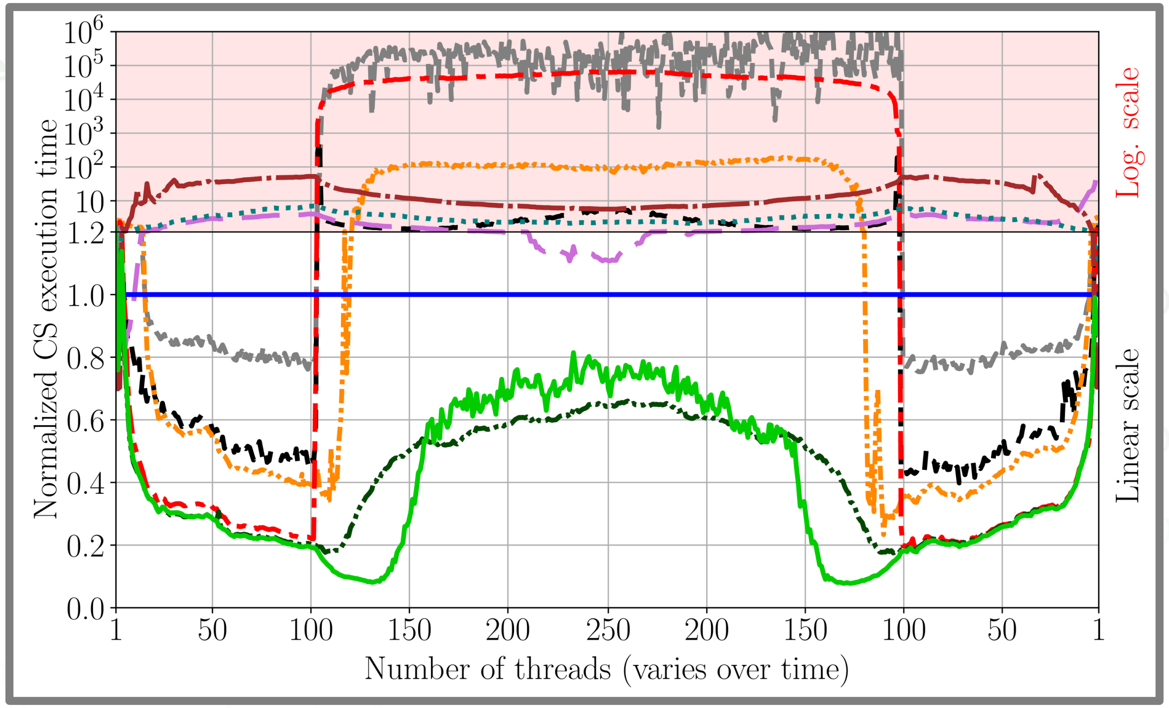

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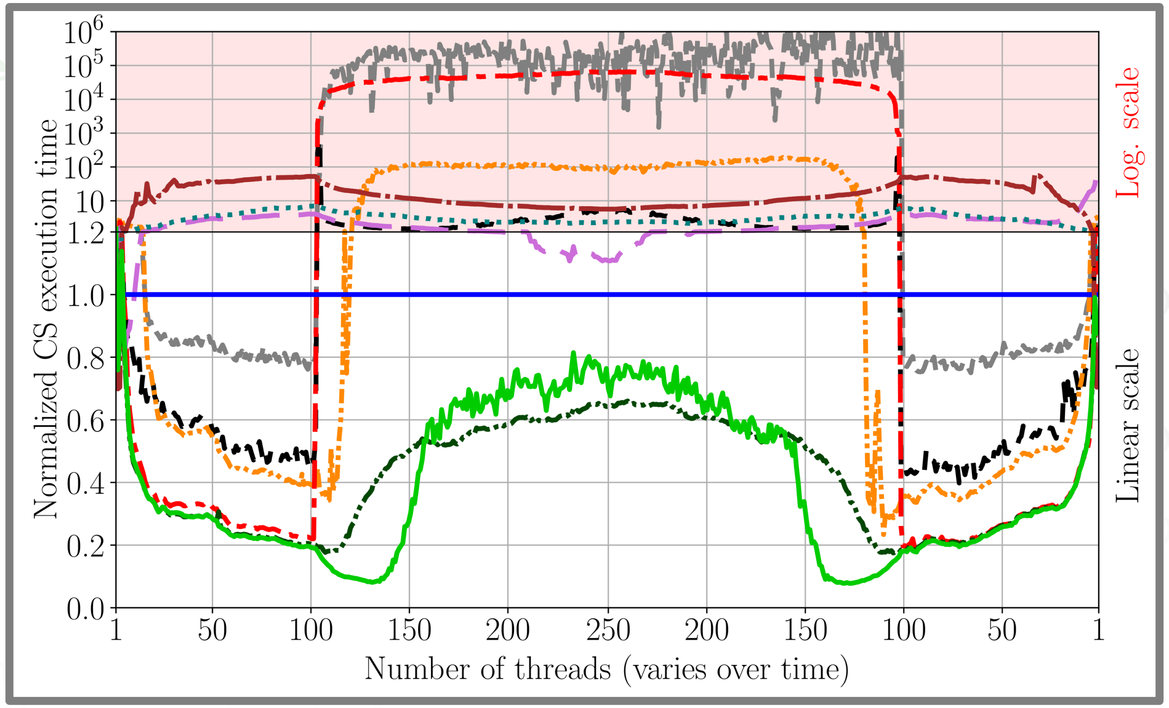
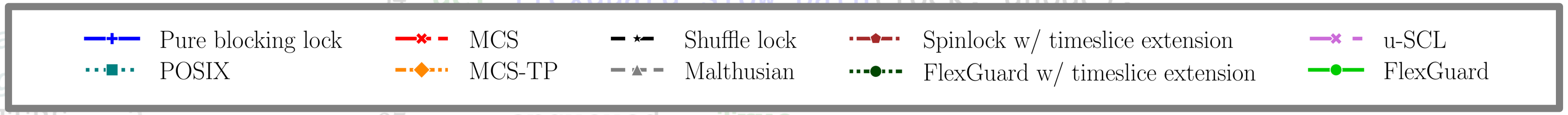
  - Recently proposed Linux timeslice extension: complementary



Conclusion



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    - First non-heuristic approach, thanks to eBPF!
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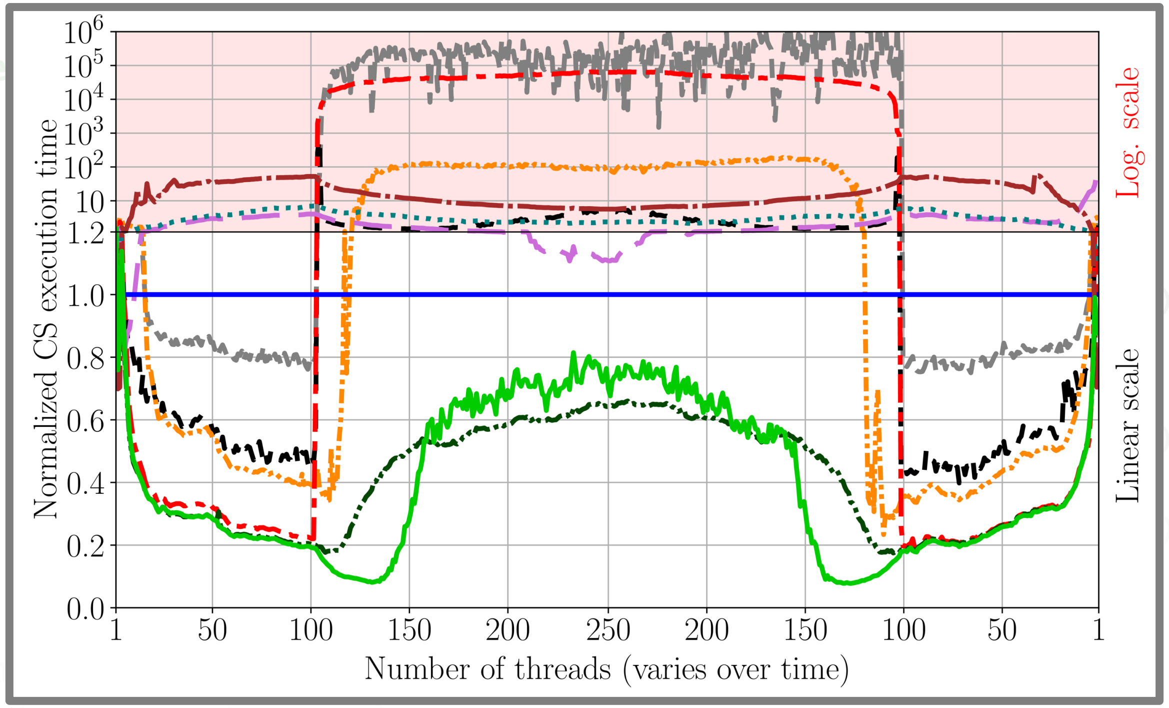

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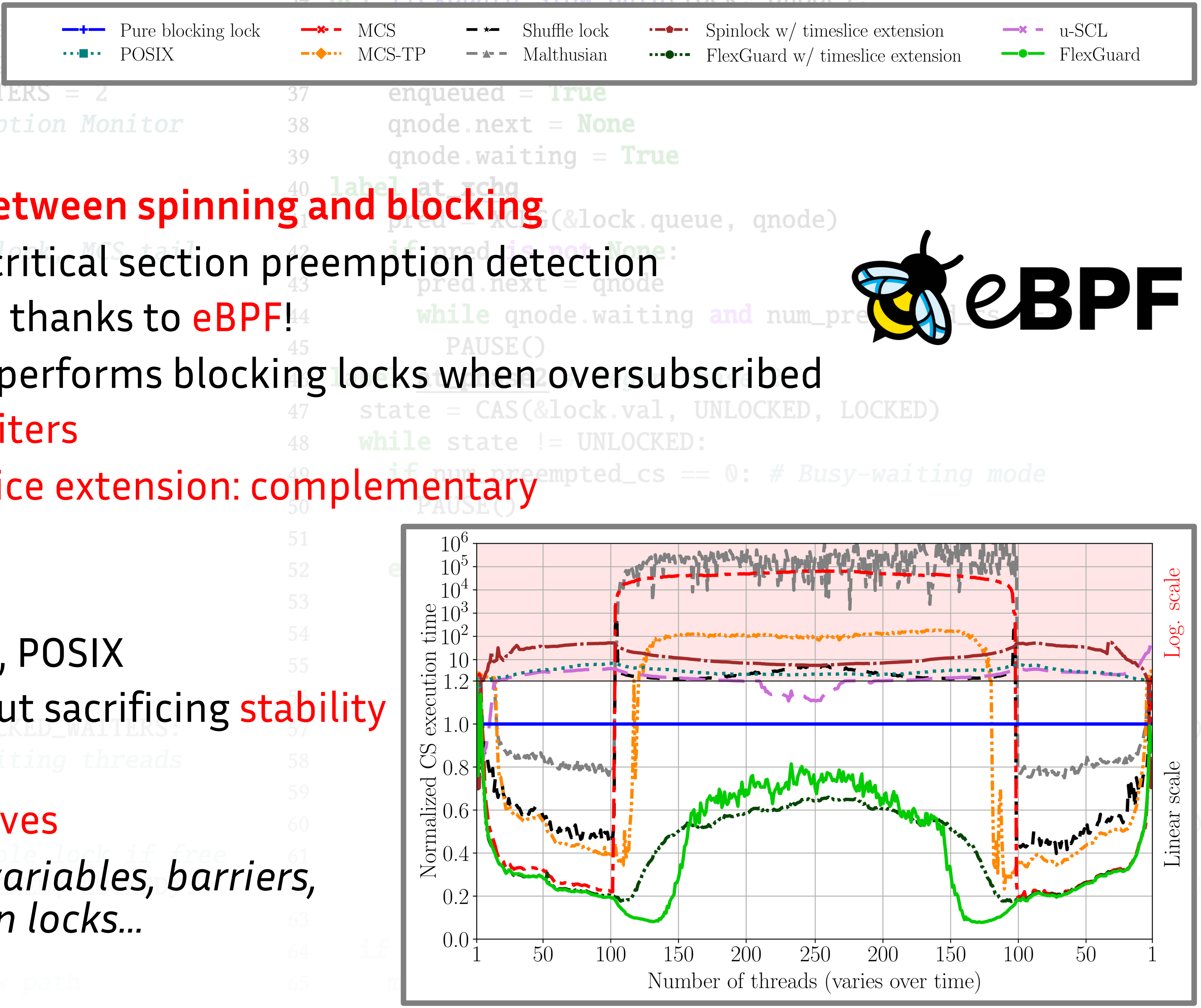

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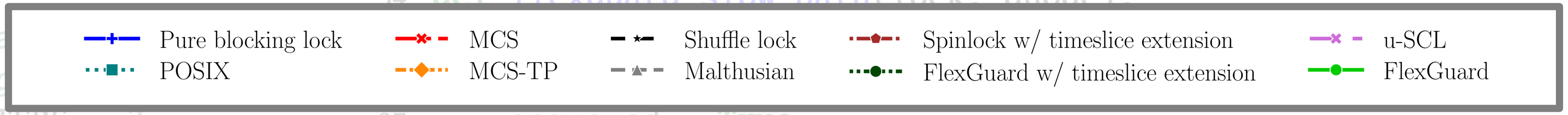

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